84-2003

Office-Supreme Court, U.S.
FILED
JUN 26 1985
ALEXANDER L. STEVAS,
CLERK

No.

In the
SUPREME COURT OF THE UNITED STATES

October Term 1984

BERWYN E. ETTER,
Petitioner,

vs.

COMMISSIONER OF PATENTS AND TRADEMARKS,
Respondent,

ANTHONY E. B. GOODFELLOW,
Intervenor.

On Petition to the United States Supreme Court for Writ of Certiorari to the Court of Appeals of the Federal Circuit.

PETITION FOR A WRIT OF CERTIORARI

Donald H. Zarley
ZARLEY, McKEE, THOMTE,
VOORHEES & SEASE
2400 Ruan Center
Des Moines, Iowa 50309
515-288-3667
ATTORNEYS FOR PETITIONER

Petitioner, Berwyn E. Etter, prays that a writ of certiorari issue to review the judgment in case 84-1213 of the United States Court of Appeals for the Federal Circuit, February 27, 1985.

THE QUESTIONS PRESENTED FOR REVIEW.

A. Did the lower court err by concluding that the statutory presumption of validity (28 U.S.C. §282) is not applicable to reexamination proceedings before the United States Patent and Trademark Office.

B. Did the lower court's decision that 28 U.S.C. §282 has no application in reexamination proceedings deprive Appellant of property without due process of law all in violation of the United States Constitution Amendment V.

C. Did the lower court err in concluding that the Etter Patent No. 4,133,034 is nonpatentable under 35 U.S.C. §103 in view of the prior art.

LIST OF ALL PARTIES TO THE PROCEEDING.

Appellant:	Berwyn E. Etter.
Appellee:	Commissioner of Patents and Trademarks.
Intervenor:	Anthony E. B. Goodfellow.

TABLE OF CONTENTS

		Page
I.	References to Official and Unofficial Reports of Opinions Delivered Below.	1
II.	Statement of the Grounds on Which The Jurisdiction of This Court is Invoked.	1
III.	Constitutional Provisions and Statutes Involved.	2
	A. U.S. Constitution - Amendment V.	2
	B. 35 U.S.C. §282.	3
	C. 35 U.S.C. §§301 - 307.	3
IV.	Statement of the Case.	3
	A. Nature of the Case.	3
	B. Course of the Proceedings.	4
V.	Argument.	6
	A. Introduction.	6
	B. The Court Erred In Concluding That "§282 Has No Application In Reexamination Proceedings."	8

Page

C. The Court's Decision "That §282 Has No Application in Re-examination Proceedings" Has The Legal Effect Of Depriving Petitioner of Property Without Due Process Of Law All In Violation Of The United States Constitution, Amendment V. 10

D. The Lower Court Erred In Concluding That The Etter Patent No. 4,133,034 Is "Nonpatentable Under 35 U.S.C. §103 In View Of The Prior Art. 16

E. Conclusion. 22

TABLE OF AUTHORITIES

	Page
American Hoist & Derrick Co. v. Sowa & Sons, Inc., 725 F.2d 1350, 1358-59 (Fed. Cir. 1984)	16
Andersen, In re, 743 F.2d 1578 (Fed. Cir. 1984)	11
Etter, In re, 756 F.2d 852, 225 U.S.P.Q. 1 (Fed. Cir. 1985)	1
Graham v. John Deere Co., 383 US 1 (1966)	17
Iowa State University Research Foundation, Inc. v. Sperry Rand Corp., 444 F.2d 406, 409 (4th Cir. 1971)	12
Lindemann Maschinenfabrik v. American Hoist and Derrick, 730 F.2d 1452, 1459 (Fed. Cir. 1984)	9
Patlex Corp. v. Mossinghoff, 758 F.2d 594, 225 U.S.P.Q. 243 (Fed. Cir. 1985)	21
Perkin-Elmer Corp. v. Computer-vision Corp., 732 F.2d 888, 894 (Fed. Cir. 1984)	16
Raytheon Co. v. Roper Corp. 724 F.2d 951, 960 (Fed. Cir. 1983)	16

CONSTITUTION

	Page
U.S. Constitution - amend. V	2, 13

STATUTES

28 U.S.C. §1254 (1966)	2
28 U.S.C. §1295 (1984) (Effective Oct. 1, 1982)	4
28 U,S.C. §2101(c) (1982)	2
35 U.S.C. §103 (1984)	16
35 U.S.C. §261 (1984)	12
35 U.S.C. 282 (1984 Supp. 1984)	2, 7, 8, 9
35 U.S.C. §§ 301-307 (1984) (Effective July 1, 1981)	2, 8, 12

I. REFERENCES TO OFFICIAL AND UNOFFICIAL REPORTS OF OPINIONS DELIVERED BELOW.

The decision of the Board of Appeals in the United States Patent Office dated February 21, 1984; and the Order on Rehearing of the Court of Appeals for the Federal Circuit dated March 25, 1985, have not been officially or unofficially reported or published at this time. The decision of the Court of Appeals for the Federal Circuit dated February 27, 1985, is officially published at 756 F.2d 852, 225 U.S.P.Q. 1 (Fed. Cir. 1985) (in banc). The decision of the lower court and the order on rehearing appear in the accompanying Appendix.

II. STATEMENT OF THE GROUNDS ON WHICH THE JURISDICTION OF THIS COURT IS INVOKED.

The date of the judgment sought to be reviewed was February 27, 1985, which was issued as a Mandate on April 4, 1985.

The date of an order respecting a rehearing was March 25, 1985.

The statutory provisions believed to confer on this court jurisdiction to review the judgment in question by writ of certiorari is 28 U.S.C. §1254 and 28 U.S.C. §2101(c).

III. CONSTITUTIONAL PROVISIONS AND STATUTES INVOLVED.

A. U.S. Constitution - Amendment V.

> "No person shall be held to answer for a capital, or otherwise infamous crime, unless on a presentment or indictment of a Grand Jury, except in cases arising in the land or naval forces, or in the Militia, when in actual service in time of War or public danger; nor shall any person be subject for the same offence to be twice put in jeopardy of life or limb; nor shall be compelled in any criminal case to be a witness against himself, nor be deprived of life, liberty, or property, without due process of law; nor shall private property be taken for public use, without just compensation."

B. 35 U.S.C. §282 (second paragraph only).

"A patent shall be presumed valid. Each claim of a patent (whether in independent, dependent, or multiple dependent form) shall be presumed valid independently of the validity of other claims; dependent or multiple dependent claims shall be presumed valid even though dependent upon an invalid claim. The burden of establishing invalidity of a patent or any claim thereof shall rest on the party asserting such invalidity."

C. 35 U.S.C. §§301 - 307 (pertinent portions thereof are contained in the accompanying Appendix).

IV. STATEMENT OF THE CASE.

A. Nature of the Case.

This is a petition for a writ of certiorari from the decision of The United States Court of Appeals for the Federal Circuit in the matter of ex parte Berwyn E. Etter, Appeal No. 84-1213 which was rendered on an in banc opinion on February 27, 1985. That appeal involved the

reexamination rejection of Etter Patent No. 4,133,034 which issued on January 2, 1979, on a Method and Means of Assimilating Utility Meter Data. The basis for jurisdiction of the Court of Appeals for the Federal Circuit was 28 U.S.C. §1295.

B. Course of the Proceedings.

The patent application of the Etter patent No. 4,133,034 was filed on July 27, 1977, and issued January 2, 1979. The request for reexamination was filed on February 4, 1982, and a final rejection was entered by the Examiner against the claims on December 10, 1982.

The matter came on for hearing before The Board of Appeals on January 26, 1984, and on February 21, 1984, The Board of Appeals rendered its decision

and upheld the Examiner's rejection of the Etter claims.

The decision of The Board of Appeals was appealed to the United States Court of Appeals for the Federal Circuit which rendered a decision on February 27, 1985. That court on its own initiative decided the case in banc, and in a split decision, concluded that the statutory presumption of validity of a patent under 35 USC §282 was not applicable to re-examination procedings. The decision of that court upheld the decision of The Board of Appeals. A concurring opinion by Judges Nies, Smith, and Bissell disagreed with the majority, and contended that the statutory presumption of validity of United States patents should be applicable in reexamination proceedings.

A Petition for In Banc Rehearing was denied on March 25, 1985.

V. ARGUMENT.

A. Introduction.

Petitioner asserts that the lower court has erroneously deprived Petitioner of the statutory presumption of validity under 35 U.S.C. §282. Petitioner further believes that had the statutory presumption of validity remained in place, the lower court would have been barred from finding the Etter patent No. 4,133,034 to be nonpatentable over the new prior art which was at best cumulative if not inferior to the prior art originally cited in the granting of the Etter patent.

The decision of the lower court has disenfranchised the patent system

from the long-standing statutory presumption of validity which has heretofore always existed. This presumption has previously always placed the burden of establishing invalidity of a patent "on the party asserting such invalidity" (35 U.S.C. §282) and this had to be done by clear and convincing evidence. Now, under the lower court's decision, as pointed out by the "dissent" in the so-called concurring opinion, the "obvious strategy of an infringer would be to force the patentee back to the PTO where the patentee's presumptive advantage, as well as claimed construction advantage, is eliminated." (Appendix p. 24). Further, "the denial of a presumption of validity gives carte blanche to the Office to 'second guess' the original allowance on the basis of

the art originally considered or, at least, not materially different." (Appendix p. 28). Thus, the public has an overwhelming interest in the dissection of the patent system which has taken place, and this Court's review of the matter is warranted.

B. The Court Erred In Concluding That "§282 Has No Application In Reexamination Proceedings."

The lower court's above conclusion is at odds with the unqualified statute, 35 U.S.C. §282, which states in part:

"A patent shall be presumed valid."

There is no qualification in that statute that exempts this presumption from administrative proceedings and limits it to patents involved in judicial proceedings. The reexamination statues (35 U.S.C. §§301-307) also fail to impose any limitation on the presumption. The lower court's

decision changes the clear, literal, unqualified language of §282: "A patent shall be presumed valid." The lower court's majority opinion addresses what the law should be, but the law has not been changed. Until it is, all issued patents must be presumed to be valid wherever they are found (except in a reissue application which is an obvious exception).

The lower court has said previously, in discussing §282, that:

> "Courts are not, of course, at liberty to repeal a statute, or to legislate conditions diminishing its effect." Lindemann Maschinenfabrik v. American Hoist and Derrick, 730 F.2d 1452, 1459 (Fed. Cir. 1984).

The majority decision altered the §282 statute and without question, the decision "diminishes its effect." If §282 does not apply to all issued patents in all administrative and judicial proceed-

ings, Congress, and not the lower court, should have made this change. The lower court's majority opinion does not just interpret §282; rather, this decision changes both the effect and literal meaning of the statute.

A construction of §282 consistent with that of the concurring opinion is therefore respectfully requested.

C. The Court's Decision "That §282 Has No Application In Reexamination Proceedings" Has The Legal Effect Of Depriving Petitioner Of Property Without Due Process Of Law All In Violation Of The United States Constitution, Amendment V.

As the reexamination of the Etter patent proceeded through the PTO, §282 and its presumption of validity existed without legislative or judicial qualification. Petitioner's position throughout that proceeding had been that because of the existence of §282, the high

standard of evidence to establish unpatentability had to be maintained, and cumulative or less pertinent art (Azure) was not effective to overcome the presumption of validity. The proceeding was tried by Petitioner with §282 fully in place.

The Court's decision in In re Andersen, 743 F.2d 1578 (Fed. Cir. 1984), was interpreted both by Petitioner and Respondent to indicate that the §282 presumption existed in reexamination proceedings. This Court's decision in the instant case changes the atmosphere in which the proceedings below were tried, for now the lower court has clarified or overruled Andersen, and has trimmed the scope of §282 by holding that the presumption exists only in judicial proceedings but not

in administrative reexamination proceedings. That decision narrows the property right that Petitioner had in his issued United States Patent for it has taken away a part of the presumption of validity that existed without qualification when the patent issued on January 2, 1979.

An issued patent has the attributes of personal property (35 USC §261).

> "The patentee has a vested property right that can be cancelled, revoked or annulled only by judicial proceedings that afford due process of law." Iowa State University Research Foundation, Inc. v. Sperry Rand Corp., 444 F.2d 406, 409 (4th Cir. 1971). (emphasis supplied).

The Etter patent issued on January 2, 1979, well before the reexamination statutes (35 USC §§301-307) became law in December of 1980, and there was no limitation on the statutory presumption of validity that enveloped that patent on the date that it

issued. Nor did the enactment of the reexamination statutes in 1980 qualify that presumption by any express or implied language.

The United States Constitution, Amendment V, states in part:

> "No person shall be ... deprived of life, liberty, or property, without due process of law; ...." (emphasis supplied).

The property right granted Etter on January 2, 1979, with the unqualified presumption of validity has now been removed, and Etter and others now possess patents that have only a qualified presumption of validity. Etter's property right in nis United States Patent with an unqualified presumption of validity has been partially removed by the lower court's determination that the presumption does not exist in reexamination proceedings.

Moreover, Etter lost this property right without due process of law, for the evidence in the proceeding below was submitted on the basis of the existence of the unqualified statutory presumption, and was not tried under established legal precedent that the presumption did not exist in such proceedings. Nor has Petitioner been heard in a judicial proceeding as to why he should not be disenfranchised from the unqualified property right which he had before either the reexamination statutes or the lower court's decision became effective.

Further, if the reexamination statutes compel a conclusion that the §282 presumption does not exist in reexamination proceedings, they must therefore be unconstitutional because they deprive

patentees of a property right without due process of law. It is Petitioner's position that these statutes do not compel such a construction of §282, and that it was the lower court's decision and not the reexamination statutes which have deprived Petitioner of his property without due process. Obviously, if the lower court decision stands, the question remains as to the constitutionality of these statutes which in that event do serve to deprive all patentees of their unqualified presumption of validity granted under §282.

Accordingly, this Court is urged either to conclude that the §282 presumption of validity applies to reexamination proceedings, or conversely, to hold that the reexamination statutes are unconstitutional as depriving patentees of a property right without due

process of law.

D. The Lower Court Erred In Concluding That The Etter Patent No. 4,133,034 Is "Nonpatentable Under 35 U.S.C. §103 In View Of The Prior Art".

The lower court has concluded that the Etter patent is invalid over the prior art patents of Ambrosio (original art) and Azure (new uncited art). If this is a correct conclusion, it must have been established by "clear and convincing evidence" if the Etter patent does enjoy the presumption of validity under §282. Perkin-Elmer Corp. v. Computervision Corp., 732 F.2d 888, 894 (Fed. Cir. 1984), American Hoist & Derrick Co. v. Sowa & Sons, Inc., 725 F.2d 1350, 1358-59 (Fed. Cir. 1984), Raytheon Co. v. Roper Corp. 724 F.2d 951, 960 (Fed. Cir. 1983). If Azure is more pertinent than the originally cited patent to Jones, and if the

greater pertinency of Azure is established by "clear and convincing evidence", the lower court's decision is proper. But the lower court has overlooked crucial evidence that shatters any reasonable conclusion that Azure is clearly and convincingly more pertinent than Jones.

Under Graham[1], the differences between the claims and the prior art needed to be determined. The missing link in the originally cited Ambrosio patent was the electronic storage or memory. The Jones patent, originally cited, revealed a small hand-held computer which had both electronic memory and the ability to calculate. The original Examiner could have said that it would be obvious for one having

---

[1] Graham v. John Deere Co., 383 U.S. 1 (1966).

ordinary skill in the art to combine the electronic memory concept of Jones with Ambrosio. He did not, and the Etter claims were allowed.

The newly cited patent to Azure also shows electronic memory, but no ability to calculate. But Azure does describe some prior art uses of electronic notebooks (Appendix p. 122, cols. 1 and 2), which only gather data, (as distinguished from "processing" data); and Azure relates that "in a typical meter reading application" (Appendix, p. 122, Col. 1, line 47), the operator at the end of the collection period would transmit "the fixed data and variable data for each meter" to a computer (lines 58-60).

So the question is: Which is more pertinent -- the Jones device with

electronic memory and calculating ability; or Azure with electronic memory without calculating ability, and a recital of prior art electronic notebooks being used to collect (not calculate) meter data?

It was error for the lower court to dismiss the comments in the Gray affidavit (Appendix,p. 145), as "merely opinions unsupported by facts and thus entitled to little or no weight." (Majority opinion, p. 16, Appendix p. 16). It was the burden of the Patent and Trademark Office to establish that Azure was more pertinent than Jones. The Patent and Trademark Office submitted nothing but arguments based on Azure's description of the prior art. Even if it is argued that Mr. Gray's affidavit is not overwhelmingly persuasive, there is no evidence, much less, clear and convincing evidence, that contradicts

paragraph 5 of the Gray affidavit.

No witness, no affidavit, and no evidence disputed Mr. Gray. No one having ordinary skill in the art disagreed with his conclusions. Yet the lower court has in effect concluded that Mr. Gray was either wrong or failed to justify his conclusions. It was not Appellant's burden to show by clear and convincing evidence that Mr. Gray's point of view was correct, it was the burden of the PTO to establish the contrary. How one (Mr. Gray) having ordinary skill in the art perceives Azure must be more convincing than how Azure is perceived by the Examiner, counsel or jurists.

The evidence revealed that one skilled in this art was conversant with both computer and meter reading (Ambrosio affidavit, Appendix p. 144). It is

unrealistic to conclude that such a person, immersed in the mysteries of electronic memory, would have overlooked the teachings of the state-of-the-art data processer of Jones, but would have been struck by the prior art dicta of the obsolete Azure data collector. It is feared by Petitioner that the Examiner, the Board and the lower court felt that the Etter claims should not have been allowed over Ambrosio and Jones, and are rushing to combine Azure to correct this mistake on the fragile and unrealistic reasoning that Azure is more pertinent than Jones. If the presumption of validity had been present, the clear and convincing rule would have been in effect, and the Azure patent could not then serve to strike down the Etter patent - particularly in the face of the Gray affidavit.

Subsequent to the decision below, the lower court has proceeded to follow its newly established precedent that the statutory presumption of validity under 35 USC §282 does not exist in reexamination proceedings. See Patlex Corp. v. Mossinghoff, 758 F.2d 594, 225 U.S.P.Q. 243 (Fed. Cir. 1985).

E. Conclusion.

The lower court has rendered a decision on a clear federal question which is in direct conflict with the clear and unqualified language of 35 U.S.C. §282. If the unqualified language and meaning of the statute is to be changed, it should be done by Congress and not by the courts. Thus, the decision below calls for an exercise of this Court's power of supervision, and certiorari should be granted to rectify this substantial encroachment on the patent

laws and the patent system of the United States.

Respectfully submitted,

BERWYN E. ETTER

By _____
Donald H. Zarley

ZARLEY, McKEE, THOMTE,
VOORHEES & SEASE
2400 Ruan Center
Des Moines, Iowa 50309
515-288-3667
ATTORNEYS FOR PETITIONER

PROOF OF SERVICE

I hereby certify that on this 24th day of June, 1985, three copies of this Petition and the accompanying Appendix are being mailed by First Class Mail with proper postage affixed to:

Solictor General, Department of Justice, Washington, D.C. 20530

Commissioner of Patents and Trademarks
c/o Thomas E. Lynch, Associate Solictor,
United States Patent and Trademark Office,
Post Office Box 15667, Arlington, VA 22215

Anthony E. B. Goodfellow, Intervenor
c/o Fleit & Jacobson,
2033 M Street, N.W.,
Washington, D.C. 20036

_____
Donald H. Zarley
ATTORNEY FOR PETITIONER

84-2005

Office-Supreme Court, U.S.
FILED
JUN 26 1985
ALEXANDER L. STEVAS,
CLERK

No.

In the
SUPREME COURT OF THE UNITED STATES

October Term 1984

BERWYN E. ETTER,
Petitioner,

vs.

COMMISSIONER OF PATENTS AND TRADEMARKS,
Respondent,

ANTHONY E. B. GOODFELLOW,
Intervenor.

On Petition to the United States Supreme Court for Writ of Certiorari to the Court of Appeals of the Federal Circuit.

APPENDIX

Donald H. Zarley
ZARLEY, McKEE, THOMTE,
VOORHEES & SEASE
2400 Ruan Center
Des Moines, Iowa 50309
515-288-3667

ATTORNEYS FOR PETITIONER

EDITOR'S NOTE

THE FOLLOWING PAGES WERE POOR HARD COPY AT THE TIME OF FILMING. IF AND WHEN A BETTER COPY CAN BE OBTAINED, A NEW FICHE WILL BE ISSUED.

APPENDIX

TABLE OF CONTENTS

	PAGE NO.
Federal Circuit Decision	1-30
Federal Circuit Decision on Rehearing	31
Etter Patent	32-37
Ambrosio Patent	38-56
Jones et al. Patent	57-95
Azure et al. Patent	96-140
Reexamination Statutes 35 U.S.C. §§301-307	141-143
Ambrosio Affidavit	144
Gray Affidavit	145-149

United States Court of Appeals for the Federal Circuit

IN RE BERWYN E. ETTER,) No. 84-1213
)
Appellant.) Reexamination No. 90/000154

DECIDED: February 27, 1985

Before MARKEY, Chief Judge, FRIEDMAN, RICH, DAVIS, BALDWIN, KASHIWA, BENNETT, MILLER, SMITH, NIES, NEWMAN, and BISSELL, Circuit Judges.

MARKEY, Chief Judge.

Appeal from a decision of the Board of Appeals (board) of the United States Patent and Trademark Office (PTO) affirming the examiner's final rejection in a reexamination proceeding of claims 1 through 9, all of the claims of United States Patent No. 4,133,034 (the '034 patent), issued January 2, 1979 to Berwyn E. Etter, as nonpatentable under 35 U.S.C. § 103 in view of prior art. We affirm.

Background

The '034 patent concerns a method and device for assimilating utility meter data at meter locations. Anthony Goodfellow, who had applied for and been refused a license under the '034 patent, filed a patent application on a utility meter reading device, copying the claims of the '034 patent to provoke an interference.[1/] The examiner refused to institute

---

1/ The '034 patent is involved in a civil action filed against a third party (M.D. Fla., Civil Action No. 81-1009. Cir. T-H). That action has been stayed, and an interference involving Etter and that party has been dissolved, in light of the examiner's determination that the claims are unpatentable. Thus the outcome here could affect a civil action and two interferences.

an interference because he found Goodfellow's claims unpatentable in view of U.S. Patent No. 3,932,730 (Ambrosio), U.S. Patent No. 4,016,542 (Azure), and U.S. Patent No. 4,115,870 (Lowell). On February 4, 1982, Goodfellow requested reexamination of the '034 patent, citing that prior art. That request was granted, and, on August 13, 1982 the examiner, having completed an ex parte examination, declared all claims of the '034 patent nonpatentable. Etter asserts that all of the claims stand or fall together.

Claim 1 is representative:

> A method of assimilating utility meter data at the meter locations, comprising,
>
> accumulating on an input information electronic storage means customer profile information for a plurality of meter customers, said profile information including the customer identity and account information,
>
> placing said input information electronic storage means in a portable computer capable of being manually carried to the site of a given meter, said portable computer having an output information storage means and having the capability of updating, printing and presenting various of said customer profile information for said meter customers before and after receiving current customer profile information,
>
> actuating said computer to segregate and to visually present from the customer profile information for a plurality of meter customers stored on said input information electronic storage means at least the meter number and customer identity information of a given meter customer,
>
> imposing into said computer the current meter reading of said given meter customer at the site of the meter being read,

actuating said computer to calculate the charge for utility usage based upon the previous meter reading and said current meter reading,

actuating said computer to print a bill for said meter customer at the site of said meter based upon said calculation and imposing on said output information storage means the updated customer profile information,

and depositing said bill at the service address of said given meter customer.

The Examiner's Rejection on Reexamination

The examiner held that the subject matter of the '034 claims would have been obvious in view of Ambrosio, which discloses the use of cards as input information storage means, and Lowell, which teaches use of random access memory (RAM) as an input information electronic storage means for storing customer information (identity, account information, etc.) for a plurality of customers, or alternatively, in view of Ambrosio and Azure, which teaches use of a solid state memory as an input information electronic storage means for storing customer information for a plurality of customers.

Finding that the environment of use for the devices of Ambrosio, Azure, Lowell, and the '034 patent (viz. on-site utility meter reading) was the same, and that Azure and Lowell discuss their inventions as being improvements over systems of the Ambrosio type, the examiner concluded that it would have been obvious to employ the memory system of either Azure or Lowell (i.e., solid state devices such as RAMs or ROMs) in place of the input information storage device taught by Ambrosio (i.e., billing cards). In effect, the rejection

rested on the view that the teachings of Ambrosio and Azure or of Ambrosio and Lowell would have made the claimed inventions of the '034 patent obvious.

The examiner accepted Etter's contention that the '034 patent enjoyed a statutory presumption of validity, 35 U.S.C. § 282, during reexamination, but viewed the presumption as having been overcome. Further, he said the presumption had been weakened by prior art (Azure and Lowell) not earlier cited to nor considered by the PTO.

Azure and Lowell were considered by the examiner as not "merely cumulative" of the prior art cited during the original prosecution, but were clearly more pertinent because they taught use of input information electronic storage means to store customer meter information for a plurality of utility customers.

The Board's Opinion

On appeal to the board, as before this court, Etter urged three grounds for reversal: (1) that the presumption of validity attaches in reexamination proceedings, and the examiner failed to carry the heavier burden thus imposed; (2) that Azure was obsolete technology, and thus constituted less pertinent art than that cited to the examiner during prosecution;[2/] and (3) that affidavits of Ambrosio and

---

2/ Etter filed a Rule 131 affidavit of prior inventorship in respect of Lowell. The examiner withdrew Lowell, but held that Ambrosio in view of Azure remained sufficient to support rejection of all claims. Etter asserts that the issue on appeal is whether the claimed inventions would have been obvious under 35 U.S.C. 103 on Ambrosio in view of Azure.

Gray showed that the invention of the '034 patent would not have been obvious.

Respecting the presumption of validity, the board noted numerous reasons for holding that it did not attach to claims undergoing reexamination. Saying that the burden of showing nonpatentability is the same on the examiner in any examination, and the board did not see how that burden would be increased in a reexamination proceeding. It further held that the evidence was such as to require affirmance of the rejection because it would sustain the examiner's burden, regardless of whether the presumption was or was not applied.

Concerning Azure, the board agreed with the examiner that it was more pertinent than the art considered during the initial prosecution, and concluded that "the collective teachings of Ambrosio and Azure would have provided a much stronger suggestion for combining the teachings to provide the subject matter" of the invention than would the teachings of the earlier cited art.

The board considered the Ambrosio and Gray affidavits unpersuasive because they showed "a total lack of appreciation of the legal concept of obviousness."[3/]

3/ As intervenor, Goodfellow filed a brief on this appeal, arguing strenuously for non-application of a presumption of validity to claims undergoing examination and reexamination. His brief also supported the board's view of the prior art and the affidavits.

Issues

(1) Must the presumption of validity, 35 U.S.C. § 282, be applied to claims involved in reexamination proceedings?

(2) Did the board err in affirming the examiner's rejection?

OPINION

(A) Presumption of Validity

Etter's basic contention -- that § 282 must be applied in reexamination proceedings -- misconstrues the purposes for which that statute and the reexamination statutes were enacted. Review of the statutes, legislative history, regulations, and case law compels the view that § 282 is not applicable to claims about which "a substantial new question of patentability," 35 U.S.C. § 305, is under consideration in a reexamination proceeding. Though the board decision here would be correct in any event, we discuss the issue because of its foundational relationship to Etter's appeal and the need for clarification of guidance offered the board and bar.

Though the board and intervenor stated strong bases for denying applicability of the presumption in reexamination proceedings, the board did recognize that it must in any event show a basis for its rejection of claims in any type of examination. Apparently for that reason, the solicitor indicated a willingness to accept applicability of § 282 in reexamination proceedings. It is true that the question has "tempest in a teapot" overtones, for the PTO will reject or cancel claims it considers unpatentable, as is its duty,

whether § 282 is or is not considered applicable. The need for clarity in the law and for avoidance of unnecessary disputes, however, has prompted this court to consider the question in banc.

Section 282 provides that "[t]he burden of establishing invalidity of a patent or any claim thereof shall rest on the party asserting such invalidity." (Emphasis added.). As this court noted in Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 718 (Fed. Cir. 1983):

> The presumption, like all legal presumptions, is a procedural device, not substantive law. It does require the decisionmaker to employ a decisional approach that starts with the acceptance of the patent claims as valid and that looks to the challenger for proof of the contrary. Thus the party asserting invalidity not only has the procedural burden of proceeding first and establishing a prima-facie case, but the burden of persuasion on the merits remains with that party until final decision . . . . With all evidence in, the trial court must determine whether the party on which the statute imposes the burden of persuasion has carried that burden. [Emphasis added.]

713 F.2d at 1534, 218 USPQ at 875.

The foregoing description in Stratoflex coincides with the inclusion of § 282 in Chapter 29 of title 35, entitled "Remedies for Infringement of Patent, and Other Actions". Both recognize that the presumption is operative to govern procedure in litigation involving validity of an issued patent. A statute setting rules of procedure and assigning burdens to litigants in a court trial does not automatically become applicable to proceedings before the PTO. Nor can it acquire an independent evidentiary role in any proceeding.

As said in the legislative history of Chapter 30 of title 35 ("Prior Art Citations to Office and Reexamination of Patents"), reexamination "will permit any party to petition the patent office to review the efficacy of a patent, following its issuance, on the basis of new information about pre-existing technology which may have escaped review at the time of the initial examination of the application." House Report No. 66-1307, 96th Cong., 2d Sess. (1980), 3-4, reprinted in 1980 U.S. Code Cong. & Ad. News 6460, 6462 (emphasis added). Reexamination is thus neutral, the patentee and the public having an equal interest in the issuance and maintenance of valid patents.

The statute, 35 U.S.C § 305, provides that "reexamination will be conducted according to the procedures established for initial examination under the provisions of sections 132 and 133 of this title." The actual reexamination is conducted ex parte. 37 CFR 1.550(a) (1983). Patent claims are reexamined only in light of patents or printed publications under 35 U.S.C. §§ 102, 103, and only new or amended claims are also examined under 35 U.S.C. §§ 112 and 132. 37 CFR 1.552; MPEP § 2258.[4/] The focus of the limited proceedings under Chapter 30

4/ If a patent owner requests reexamination, but desires consideration of wider issues, e.g., prior public use or sale, he must obtain such consideration by filing a reissue application. 37 CFR 1.552; MPEP §§ 2212, 2258. The present case involves a non-patentee requestor; it should be remembered, however, that reexamination may be a boon to patentees whose patents may be thereby strengthened, and that the actual reexamination procedure itself should be the same whoever be the requestor.

thus returns essentially to that present in an initial examination, i.e., to a time at which no presumption of validity had been created.

The innate function of the reexamination process is to increase the reliability of the PTO's action in issuing a patent by reexamination of patents thought "doubtful." House Report at 3. When the patent is concurrently involved in litigation, an auxiliary function is to free the court from any need to consider prior art without the benefit of the PTO's initial consideration. In a very real sense, the intent underlying reexamination is to "start over" in the PTO with respect to the limited examination areas involved, and to reexamine the claims, and to examine new or amended claims, as they would have been considered if they had been originally examined in light of all of the prior art of record in the reexamination proceeding. That intent is reflected in 35 U.S.C. § 303, which requires the Commissioner to determine whether "a substantial new question of patentability" has been raised, and in 35 U.S.C. § 304, which provides for initiation of reexamination by the Commissioner sua sponte.

The intent that reexamination proceedings and court actions involving challenges to validity be distinct and independent is reflected in the legislative history of § 303, which notes that denial of a request for reexamination does not deprive the requestor (if not the patent owner) "of any legal right" to contest validity in subsequent court proceedings. House Report at 6466. That "legal right" may be exercised as a matter of right, but determination of whether a "substantial new question

of "patentability" exists, and therefore whether reexamination may be had, is discretionary with the Commissioner, and, as § 303 provides, that determination is final, i.e., not subject to appeal.[5/]

That a patentee may request reexamination, and has the opportunity in the PTO of distinguishing art newly cited by the examiner, 37 CFR 1.530(c), and may amend his claims under reexamination, 35 U.S.C. § 305, further distinguish reexamination from litigation. It is of no moment that the examiner's burden of showing a basis for rejection in the examination and reexamination processes is not described in the "clear and convincing" terms applicable under § 282 to a litigant challenging validity of an issued patent. During the examination processes, allowances of claims raise no presumption and may be withdrawn. That one challenging validity in court bears the burden assigned by § 282, that the same party may request reexamination upon submission of art not previously cited, and that, if that art raises a substantial new question of patentability, the PTO may during reexamination consider the same and new and amended claims in light of that art free of any presumption, are concepts not in conflict. On the contrary,

---

5/ The inquiry occasioned by a request for reexamination is solely whether a reexamination order should issue and is not directed toward resolution of validity. The requestor's burden is simply to show a basis for issuance of the order, a burden unrelated to that assigned in § 282. A refusal of reexamination leaves untouched the § 282 presumption to which the patent is entitled in the courtroom. Similarly, a reexamination may involve only certain claims, e.g., those in litigation, and the newly cited prior art may bear no relation to other claims, to which the presumption of validity would remain attached in future litigation involving those claims.

010

those concepts are but further indication that litigation and reexamination are distinct proceedings, with distinct parties, purposes, procedures, and outcomes. In the former, a litigant who is attacking the validity of a patent bears the burden set forth in § 282. In the latter, an examiner is not attacking the validity of a patent, but is conducting a subjective examination of claims in the light of prior art.

In In re Yujiro Yamamoto, 740 F.2d 1569, 222 USPQ 934 (Fed. Cir. 1984), this court said that claims subject to reexamination will "be given their broadest reasonable interpretation consistent with the specification, and limitations appearing in the specification are not to be read into the claims." 740 F.2d at 1571, 222 USPQ at 936. That standard is applied in considering rejections entered in the course of prosecution of original applications for patent. See In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). As noted in Yamamoto:

> [a]n applicant's ability to amend his claims to avoid cited prior art distinguishes proceedings before the PTO from proceedings in federal district courts on issued patents. When an application is pending in the PTO, the applicant has the ability to correct errors in claim language and adjust the scope of claim protection as needed. This opportunity is not available in an infringement action in district court. . . .
>
> The same policies warranting the PTO's approach to claim interpretation when an original application is involved have been held applicable to reissue proceedings because the reissue provision, 35 U.S.C. § 251, permits amendment of the claims to avoid prior art. [Citation omitted.] The reexamination law . . . gives patent owners the same right . . .

740 F.2d at 1572, 222 USPQ at 936.

Claims in a reissue application enjoy no presumption of validity. In re Sneed, 710 F.2d 1544, 1550 n.4, 218 USPQ 385, 389 n.4 (Fed. Cir. 1983). Though reissue and reexamination proceedings are distinct, the focus of both is on curing defects which occurred during a proceeding in the PTO, which was responsible for original issuance of the patent.

Etter cites language in In re Andersen, 743 F.2d 1578, 223 USPQ 378 (Fed. Cir. 1984), as appearing to require application of § 282 in reexamination proceedings. At oral argument, the PTO solicitor indicated that Andersen has been understood by and accepted in the PTO as establishing that requirement.

The court in Andersen dealt with Andersen's argument that any doubt must be resolved in his favor under (1) a judicially imposed "rule of doubt," or (2) as "part of the presumption of validity." The court rejected (1), citing In re Nabor, 503 F.2d 1059, 183 USPQ 245 (CCPA 1974), and rejected (2), noting that the presumption does not embrace a rule of doubt. The court agreed with Andersen's statement that reexamination should not circumvent the burden "placed on an infringer during litigation." As above indicated, that is a truism, the litigation and reexamination processes being distinct. The court's discussion of the workings of the presumption in the face of new art, and the cases cited, all related to operation of the presumption in litigation.

Nonetheless, recognizing that Andersen may be and has been read as holding that claims must be presumed valid under § 282 in reexamination proceedings, the court has sua sponte taken this case in banc to clarify the law as set forth in this opinion.

No statutory language and no legislative history indicates any support for a requirement that the provisions of 35 U.S.C. § 282 must be applied in the consideration of claims involved in reexamination proceedings. Indeed, all available indications are to the contrary. We hold, therefore, that § 282 has no application in reexamination proceedings.

It is at best incongruous to apply a trial court procedural rule to the examination of claims in the PTO. Moreover, because this court and one of its predecessors has consistently held that the PTO examiner has the burden of showing a basis under the statute, 35 U.S.C., for each rejection, injection of the presumption into the examination process could add nothing but legalistic confusion.

This court has repeatedly pointed out that the § 282 presumption is a rule of procedure placing the burden of persuasion on him who attacks a patent's validity. There is no such attacker in a reexamination, and hence no one on whom that burden may be placed.[6/] In litigation, where a patentee cannot

---

6/ No third party is involved when reexamination is requested by the patentee or initiated sua sponte by the Commissioner. When a third party (whether or not an alleged infringer, and whether or not suit has been filed) is the requestor, that party is heard only on whether "a substantial new question" exists. Absent a "substantial new question", an alleged infringer cannot "force" a patentee back into the PTO. Contrary to indications in the concurrence, the reexamination per se of the claims is entirely ex parte. Whether a requestor, or other party, is permitted to intervene in an appeal to this court (the intervenor being thereby bound by the decision on appeal) is discretionary with this court. In all events, concentration on those instances when an alleged infringer is present at the requesting stage should not influence a decision on whether § 282 applies in the ex parte reexamination proceeding.

amend his claims, or add new claims, the presumption, and the rule of claim construction (claims shall be construed to save them if possible), have important roles to play. In reexamination, where claims can be amended and new claims added, and where no litigating adversary is present, those roles and their rationale simply vanish.

The patent right is a right to exclude. The statute, 35 U.S.C. § 261, says that "patents shall have the attributes of personal property."[7/] The essence of all property is the right to exclude, and the patent property right is certainly not inconsequential. It is, nonetheless, created by a grant from the government. When a "substantial question" exists respecting the correctness of that grant, it does not conflict but coincides with the nature of the grantee's right when the government reexamines the propriety of the grant it has made, and thereafter reaffirms the grant, substitutes a new grant (amended or new claims), or withdraws the grant in whole or in part (the last being subject to review in this court).

(B) The Merits

The examiner and the board correctly determined that: (1) Ambrosio discloses all features of Etter's claims, except "input information electronic storage means [for accumulating] customer profile information for a plurality of customers;" (2) Azure discloses that feature; (3) the overall result of the inventions of Ambrosio, Azure, and Etter is the same; and (4) Etter's claimed inventions would have been obvious in view of the collective

---

7/ A patent is not a "deed", a term normally used to describe an attribute of real property.

teachings of Ambrosio and Azure which would have provided "a much stronger suggestion for combining the teachings to provide the subject matter of claim 1" than would the prior art cited during the original prosecution.

Harking back to his § 282 argument, Etter says the claims were originally allowed over Ambrosio and Jones, and Azure is less pertinent than Jones. Azure and Jones each disclose electronic memory. The board correctly noted, however, that Azure, unlike Jones, discloses use in utility meter reading among possible uses of his input information electronic storage means and is therefore more pertinent. That Azure disclosure is not, as Etter says, mere "hearsay". Etter's arguments that Azure does not disclose calculation and does disclose obsolete technology were properly rejected as insufficiently founded. Etter admits that Ambrosio discloses calculation. Obsolescence, if established, need not necessarily defeat a reference for what it discloses in reference to a claimed invention. Further, Etter relies on the opinion affidavit of Gray for his assertion that Azure discloses obsolete technology. Etter's assertions that Azure cannot be incorporated in Ambrosio are basically irrelevant, the criterion being not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole. Orthopedic Equipment Co. v. United States, 702 F.2d 1005, 1013, 217 USPQ 193, 200 (Fed. Cir. 1983); In re Andersen, 391 F.2d 953, 958, 157 USPQ 277, 281 (CCPA 1968).

Review of the Ambrosio and Gray affidavits confirms the correctness of the board's characterization as merely representing opinions unsupported by facts and thus entitled to little or no weight. See In re Piasecki, No. 84-775 (Fed. Cir. Oct. 17, 1984), slip op. at 9-10; In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

AFFIRMED

IN RE BERWYN E. ETTER,) No. 84-1213
)
Appellant.) Reexamination No. 90/000154

NIES, Circuit Judge, with whom SMITH and BISSELL, Circuit Judges, join, concurring.

While I agree with the result reached by the majority, I disagree with the majority opinion insofar as it holds that, in a reexamination proceeding, a patent is never accorded the presumption of validity. In this case it makes no difference whether the presumption is or is not applied, as the board itself stated. The holding that the claimed invention would have been obvious over art not previously considered is fully justified, had the presumption been recognized.

This case illustrates the advantage of the new reexamination procedure. It worked here precisely as proponents of the legislation envisaged. What has resulted, however, in my view, is an easy case making bad law, not unusual with dicta. The majority decision finds a negation of the statutory presumption that is not expressed in the statute. Further, the majority opinion cannot be justified on the grounds that it is necessary to achieve the statutory objectives. Indeed, this decision can only have a chilling effect on voluntary use of the new procedure by patent owners, which was to be one of its prime objectives. H.R. Rep. No. 1307, 96th Cong., 2d Sess. 4, reprinted in 1980 U.S. Code Cong. & Ad. News 6460, 6463.

After complying with the procedures promulgated by Congress for obtaining a patent, a patent owner is in a

position comparable to the holder of a deed or title to property. 35 U.S.C. § 261 (1982); Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); Schenck v. Nortron Corp., 713 F.2d 782, 784, 218 USPQ 698, 699 (Fed. Cir. 1983). That government grant is not to be set aside unless the deciding tribunal is clearly convinced that the grant was in error, having been predicated on erroneous or incomplete facts or a wrong application of law.

The statutory provision in 35 U.S.C. § 282 is absolute:

> A patent shall be presumed valid.

Nothing in the reexamination chapter, 35 U.S.C. §§ 301-307, states otherwise.[1/] Nothing in the legislative history indicates that Congress intended a patent owner involved in reexamination to "start over" to resecure his patent. On the contrary, the chapter is directed simply to resolution of a new question of patentability under 35 U.S.C. §§ 102 or 103. Specifically, 35 U.S.C. § 304 provides:

> § 304. Reexamination order by Commissioner
>
> If, in a determination made under the provisions of subsection 303(a) of this title, the Commissioner finds that a substantial new question of patentability affecting any claim of a patent is raised, the determination will include an order for reexamination of the patent for resolution of the question. [Emphasis added.]

1/ The directive in 35 U.S.C. § 305 to follow "procedures established for initial examination under the provisions of sections 132 [PTO must give notice of rejection with reasons] and 133 [time for response]" patently have no bearing on the substantive issue here.

As explained in the legislative history:

> This "substantial new question" requirement would protect patentees from having to respond to, or participate in unjustified reexaminations. Further, it would act to bar reconsideration of any argument already decided by the Office, whether during the original examination or an earlier reexamination.

H.R. Rep. No. 1307, 96th Cong., 2d Sess. 7, reprinted in 1980 U.S. Code Cong. & Ad. News 6460, 6466.

The presumption of validity dovetails neatly with reexamination to resolve a substantial new question of patentability and its application would fit within the precedent of this court in which the presumption of validity has been defined or its effect explained in a series of decisions.[2/] Indeed, in In re Andersen, 743 F.2d 1578, 1580, 223 USPQ 378, 380 (Fed. Cir. 1984), the PTO acknowledged that the presumption of validity applied.[3/]

The presumption of validity places on the challenger of a patent the burden of coming forward with evidence to

---

2/ American Hoist & Derrick Co. v. Sowa & Sons, 725 F.2d 1350, 1358-60, 220 USPQ 763, 769-71 (Fed. Cir. 1984); Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1534, 218 USPQ 871, 875-76 (Fed. Cir. 1983); SSIH Equipment S.A. v. U.S. Int'l Trade Comm'n, 718 F.2d 365, 375, 218 USPQ 678, 687 (Fed. Cir. 1983); Solder Removal Co. v. U.S. Int'l. Trade Comm'n., 582 F.2d 628, 632-33, 199 USPQ 129, 133 (CCPA 1978).

3/ In this case, the board's position is that it makes no difference whether the presumption applies or not. In In re DeWitt, No. 581-71, slip op. at 5 (Bd. App. May 30, 1984), the appeal of which is also decided today, No. 84-1555 (Fed. Cir. Feb. 27, 1985), the board took the next step and explicitly held that the presumption did not apply to claims under reexamination.

establish facts which may lead to the conclusion that the patent is invalid. SSIH Equipment S.A. v. U.S. Int'l Trade Comm'n, 718 F.2d 365, 375, 218 USPQ 678, 687 (Fed. Cir. 1983). The challenger bears the burden of proof of such facts, as well as the ultimate burden of persuasion on the legal issue of validity. Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1534, 218 USPQ 871, 875 (Fed. Cir. 1983). The PTO acknowledges that it bears these burdens in examination of an original application or in reexamination of patent claims. The PTO does not accept, however, that the quantum of proof of facts is "clear and convincing" evidence, which this court has stated to be imposed by the presumption. SSIH, 718 F.2d at 375, 218 USPQ at 687.

Our precedent holds that the presumption of validity is not weakened or destroyed during litigation by presentation of more relevant art not considered by the PTO, but may be more easily overcome if such art is presented. American Hoist & Derrick Co. v. Sowa & Sons, 725 F.2d 1350, 1358-60, 220 USPQ 763, 769-71 (Fed. Cir. 1984). This follows from the absence of a decision on such matter by the administrative expert, the PTO examiner, to which deference must be given. Id. at 1359, 220 USPQ at 770. The situation in reexamination falls precisely within this concept. If reexamination concerns only a question of patentability not previously considered by the PTO, a fortiori, there is no prior decision to which deference is due

and the presumption can be more easily overcome. But deference should be required in reexamination with respect to a matter which was previously considered or is substantially the same, e.g., basing a rejection on a new reference which is not materially different from one which has been overcome. The legislative history quoted above expresses a clear intent, consistent with the presumption of validity, that patents are not to be examined de novo. The legislative history quoted by the majority relates only to previously unconsidered matters. However, concerning matters which are essentially the same as those previously considered which may be re-raised during reexamination, a patentee is entitled to more respect for his property than the majority decision recognizes. Indeed, the majority's analysis and certain statements in the legislative history which speak of enhancing the presumption of validity by reexamination[4/] seem to equate the presumption of validity with the presumption of administrative regularity or correctness, a concept which our precedent has specifically rejected. American Hoist, 725 F.2d at 1359-60, 220 USPQ at 770.

The majority justifies its position that the presumption does not apply in reexamination on the ground that

---

4/ See, e.g., Patent Reexamination: Hearings on S. 1679 Before the Comm. on the Judiciary, 96th Cong., 1st Sess. 1, 60 (1979) (testimony of Arthur R. Whale) ("[Reexamination] will bring the presumption of validity to the same level with respect to newly cited art.").

reexamination is an ex parte proceeding, while the presumption is appropriate only in inter partes disputes. The record in this case shows that an alleged infringer in litigation forced the reexamination, filed a brief analyzing the art in connection with its request to the PTO, filed a reply to the patent owner's objection, was served with copies of the examiner's actions and the patent owner's responses, and was permitted to intervene and brief matters in this court. The record here does not disclose that affidavits accompanied the alleged infringer's request for reexamination or his reply to the patent owner's statement, but this type of submission is allowed by such person. To characterize reexamination in its entirety as an ex parte proceeding under such circumstances, while technically correct, ignores reality. It is, in my view, more appropriate to view it here as collateral to the pending litigation, although without res judicata effect against the alleged infringer if the claims are held valid. 3 Chisum, Patents § 11.07[4][f], at 11-128 (1984).

I agree with the majority that reexamination should work in such a manner that it will be "neutral." However, the decision today, in my view, will make patent owners resistent to reexamination. The deck is stacked against them by this decision and by In re Yamamoto, 740 F.2d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984). The court has made reexamination into a proceeding which affords advantages to an infringer over his position in court.

Delay itself is an advantage to an infringer of greater economic power than the patent owner, and the lack of res judicata effect against the infringer gives that party two opportunities to attack the patent. These advantages are inherent in reexamination and must be accepted as the quid pro quo for the perceived benefits of reexamination. We need not, however, go further and, as a matter of statutory interpretation, also change the rules by which validity is to be judged to the infringer's benefit. An infringer may well have evidence which is sufficient to meet the low threshold of "a substantial new question of patentability", but not sufficiently persuasive in court to overcome the presumption of validity, including the burden of clear and convincing proof. This might be particularly true where evidence is submitted to the PTO in the form of affidavits of experts or others who thereby escape the testing of cross examination.

With respect to claim construction, claims in litigation are to be "so construed, if possible, as to sustain their validity." ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 932 (Fed. Cir. 1984), citing Klein v. Russell, 86 U.S. (19 Wall.) 433, 466 (1874); Turrill v. Michigan, S. & N.I. R.R., 68 U.S. (1 Wall.) 491, 510 (1864). Claims in reexamination, on the other hand, "will be given their broadest reasonable interpretation." In re Yamamoto, 740 F.2d at 1571, 222 USPQ at 936. Thus, claims

may be valid and infringed in court but invalid in the PTO and, a fortiori, not infringed. It is small solace to a patent owner in that situation that he may amend his claims in reexamination and secure narrower new claims. Upon amendment, his claims are subject to complete examination and an infringer has the benefit of intervening rights to the extent afforded under 35 U.S.C. § 252 pursuant to 35 U.S.C. § 307(b).

Given this court's interpretation of proper reexamination procedure, the obvious strategy of an infringer would be to force the patentee back to the PTO where the patentee's presumptive advantage, as well as claim construction advantage, is eliminated.

The majority's analysis focuses on the aspect of reexamination dealing with the threshold determination that "a substantial new question of patentability" has been raised. The majority then continues its analysis of this case as if reexamination itself is a "limited examination" directed to that question. However, our court has also analogized reexamination to reissue proceedings. In re Yamamoto, 740 F.2d at 1572, 222 USPQ at 937. In reissue, examination is not limited to the question raised by the patent owner. 37 C.F.R. § 1.176. The PTO has taken a similarly expansive view of the scope of reexamination in its regulations and in its stated operating procedures.

Reexamination, as interpreted by the PTO, is a two step process involving: (1) the determination that there is "a substantial new question of patentability", and (2) reexamination itself. The latter step is not constrained, in the PTO view, by the former. In a very real sense, once reexamination is ordered (an unreviewable decision), the patent holder "starts over" under the PTO view on all § 102 and § 103 issues with respect to all claims, amended or unamended, whether or not related to the new question.

With respect to the first step, i.e., determining whether there should be reexamination, PTO regulation 37 C.F.R. § 1.515 provides:

> § 1.515 Determination of the request for reexamination.
>
> (a) Within three months following the filing date of a request for reexamination, an examiner will consider the request and determine whether or not a substantial new question of patentability affecting any claim of the patent is raised by the request and the prior art cited therein, with or without consideration of other patents or printed publications. [Emphasis added.]

Turning to the Manual of Patent Examining Procedure (MPEP), one sees that examiners are instructed as follows, when considering a request for reexamination:

> § 2242 Criteria for Deciding Request.
>
> . . . Material new arguments or interpretations can raise "a substantial new question of patentability" as to prior art patents or printed publications already considered by the Office.

§ 2244 Prior Art on Which Determination Is Based.

> The determination whether or not "a substantial question of patentability" is present can be based upon any prior art patents or printed publications. Section 303(a) of the statute and 37 CFR 1.515(a) provide that the determination on a request will be made "with or without consideration of other patents or printed publications," i.e., other than those relied upon in the request. The examiner is not limited in making the determination to the patents and printed publications relied upon in the request. The examiner can find "a substantial new question of patentability" based upon the prior art patents or printed publications relied upon in the request, a combination of the prior art relied upon in the request and other prior art found elsewhere, or based entirely on different patents or printed publications. The primary source of patents and printed publications used in making the determination are those relied upon in the request. However, the examiner can also consider the prior art of record in the patent file from the earlier examination or a reexamination and any patents and printed publications of record in the patent file from submissions under 37 CFR 1.501 which are in compliance with 37 CFR 1.98 in making the determination.
>
> * * *
>
> Any question as to whether a substantial new question of patentability exists should be resolved in favor of granting the request for reexamination. [Emphasis added.]

With respect to the scope of the examination on reexamination, the second step, 37 C.F.R. § 1.552(a) provides:

> Patent claims will be reexamined on the basis of patents or printed publications.

No limitation is found there, or is intended, to limit reexamination to the new question of patentability which

started reexamination.[5/] In making rejections, the examiners are told in the MPEP:

> § 2256 Prior Art Patents and Printed Publications Considered by Examiner in Reexamination.
>
> The primary source of prior art will be the patents and printed publications cited in the request.
>
> The examiner must also consider patents and printed publications
>
> --cited by a reexamination requester under § 1.510
>
> --cited in patent owner's statement under § 1.530 or a requester's reply under § 1.535 if they comply with § 1.98
>
> --cited by patent owner under a duty of disclosure (§ 1.555) in compliance with § 1.98
>
> --discovered by the examiner in searching

5/ In publishing the implementing regulations, Acting Commissioner of Patents and Trademarks Tegtmeyer stated with respect to the scope of reexamination:

> The scope of the reexamination proceeding which was originally proposed has been essentially adopted in the final rules. The suggestions that the rules be broadened to include other issues have not been adopted since the other issues would unduly complicate the proceedings, raise the expense of the proceedings and raise questions whether such issues can be considered under Pub. L. 96-517.

1007 O.G. 31 (1981).

Thus, while "other" issues such as fraud, will not be considered, the only stated limitation on §§ 102 and 103 issues is that indicated above.

--of record in the patent file from earlier examination

--of record in patent file from § 1.501 submission prior to date of an order if it complies with § 1.98. [Emphasis added.]

§ 2216 Substantial New Question of Patentability.

. . . If a substantial new question of patentability is found as to one claim, all claims will be reexamined during the ex parte reexamination process. [Emphasis added.]

The MPEP example of the processing of a "typical" reexamination shows a request for reexamination of claims 1-4 of a patent (MPEP § 2214, at 2200-11); a decision that a new question is raised as to claims 1-3 and no new question as to claim 4 (MPEP § 2246, at 2200-29); and, finally, a decision (1) not to reexamine claims 1-3 because of a court decision; (2) a rejection of issued claim 4; (3) a determination of patentability of issued claim 5; and (4) a rejection of new claim 6 (MPEP § 2262, at 2200-41). Thus, issued claim 4 is lost--although no decision was made that a substantial new question of patentability existed to involve the claim in the reexamination.

Coupling this expansive view of the scope of reexamination with the denial of a presumption of validity gives carte blanche to the Office to "second guess" the original allowance on the basis of the art originally considered or, at least, not materially different. This unrestrained view of its power during reexamination was,

indeed, expressed by the board in In re DeWitt, No. 581-71, slip. op. at 5 (Bd. App. May 30, 1984), the appeal of which is also decided today, No. 84-1555 (Fed. Cir. Feb. 27 , 1985), in which the board opined:

> [T]here is no policy reason against the Office reconsidering its own work product and admit it may have made an error. . . .

This view is too simplistic. The questions of validity of patents over prior art are not clear cut. The conflicting testimony of responsible experts, which this court sees every day in the records of patent cases before it, belies the concept that determining an "error" was made will be readily apparent.[6/] The ultimate decision is a judgment call and the result may well depend on whether one starts with the view that the patent is valid or that reexamination starts on a clean slate. See American Hoist, 725 F.2d at 1358-60, 220 USPQ at 769-71 (judgment of invalidity reversed, inter alia, for failure to accord presumption of validity).

For the foregoing reasons, I believe it would be the correct and desirable interpretation of the statute to apply the presumption of validity in reexamination in the same manner

---

6/ "Federal courts have a difficult enough time trying to determine whether an invention, narrowed by the patent application procedure and fixed in the specifications which describe the invention for which the patent was granted, is patentable." Kewanee Oil Co. v. Bicron Corp., 416 U.S. 470, 492 (1973).

as in court proceedings, and I would also apply the identical standard for claim construction.7/

Alternatively, I urge the majority to limit reexamination to "resolution of the question," that is, to the "substantial new question of patentability" which caused the reexamination to be ordered, in accordance with 35 U.S.C. § 304. Nothing in the statute constrains the Commissioner, of course, from finding more than one substantial new question of patentability. However, under the statute, the Commissioner is required to make such determination. He should not merely allow reexamination to proceed in any direction at the discretion of an examiner. Clearly, reexamination was not designed to allow the PTO simply to reconsider and second guess what it has already done.

7/ Implicit in my opinion, of course, is that no presumption applies to new or amended claims.

United States Court of Appeals for the Federal Circuit

In the Matter of the Application

of

BERWYN E. ETTER, PATENT OWNER AND
ANTHONY E. B. GOODFELLOW, INTERVENOR

No. 84-1213
Reexam. No. 90/000154

O R D E R

A petition for rehearing and a suggestion for rehearing in banc having been filed in this case,

UPON CONSIDERATION THEREOF, it is Ordered by the court that the petition for rehearing be, and the same is hereby, Denied.

The suggestion for rehearing in banc is declined.

FOR THE COURT

George E. Hutchinson, Clerk

March 25, 1985
Date

CC: Ms. Thomas E. Lynch
Solicitor, U.S.Patent
and Trademark Office

United States Patent [19]

Etter

[11] **4,133,034**

[45] **Jan. 2, 1979**

[54] **METHOD AND MEANS OF ASSIMILATING UTILITY METER DATA**

[76] Inventor: Berwyn E. Etter, 368 Boca Ciega Point Blvd. So., Madeira Beach, Fla. 33708

[21] Appl. No.: 819,350

[22] Filed: Jul. 27, 1977

[51] Int. Cl.² G06K 1/00

[52] U.S. Cl. 364/464; 235/432; 364/483; 364/900

[58] Field of Search ..... 364/200, 900, 401, 403, 364/464, 483, 709; 235/152, 151.3, 151.31, 61.9 R, 61.6 R, 156; 340/149 R

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,344,408	9/1967	Singer et al.	364/900
3,590,220	6/1971	Ishida et al.	235/61.9 R
3,842,248	10/1974	Yarnell et al.	235/156
3,932,730	1/1976	Ambrosio	235/61.9 R
3,956,740	5/1976	Jones et al.	364/200
4,007,443	2/1977	Bromberg et al.	364/900
4,025,766	5/1977	Ng et al.	235/152

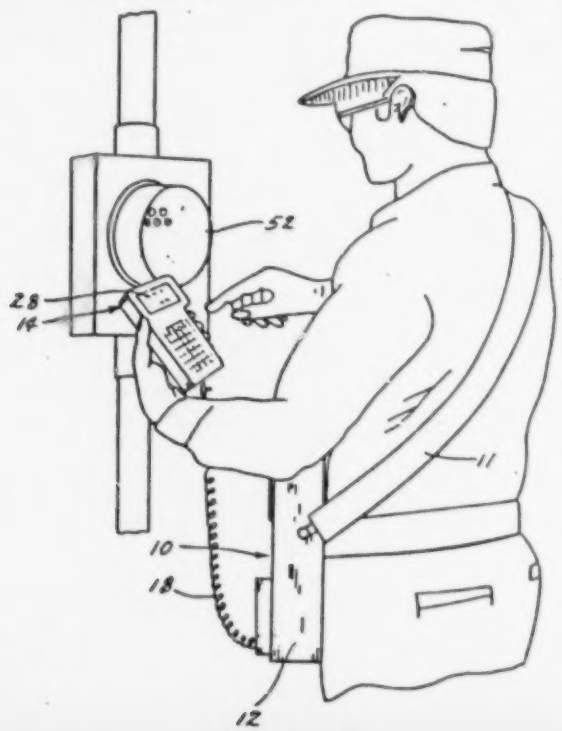
Primary Examiner—Charles E. Atkinson
Assistant Examiner—Errol A. Krass
Attorney, Agent, or Firm—Zarley, McKee, Thomte, Voorhees & Sease

[57] **ABSTRACT**

A method of assimilating utility meter data at the meter locations by accumulating on an input tape customer profile information for a plurality of meter customers, including the customer's account number, service address, meter number, customer name, previous reading date and meter reading, utility rate factors and debit/-credit transactions. The input tape is then placed in a portable computer capable of being manually carried to the site of a given meter. The portable computer has the capability of updating, printing and visually presenting various of the customer profile information before and after receiving current customer profile information. The computer is actuated to visually present at least the meter number and customer address of a given meter customer. The current meter reading is then placed in the computer which is then actuated to calculate the charge for the utility usage based upon the previous meter reading and the current meter reading. The computer is then actuated to print a bill for the meter customer, and the computer imposes on an output tape the updated customer profile information. The printed bill is then removed from the computer and deposited at the customer address.

A device for assimilating utility meter data comprising a portable computer means having a computer housing, computer circuitry, input and output tapes connected to the computer circuitry, printout means operatively connected to the computer circuitry, and a manually held control means connected to the computer housing by a flexible coupling for actuating the computer circuitry and for putting raw data into the computer means. The manual control means includes a visible message output board connected to the computer circuitry whereby the operator can visually observe certain of the information contained in the computer as said information is imposed on the output board.

9 Claims, 3 Drawing Figures



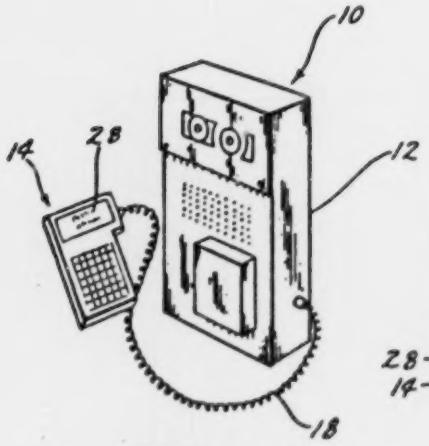


Fig. 1

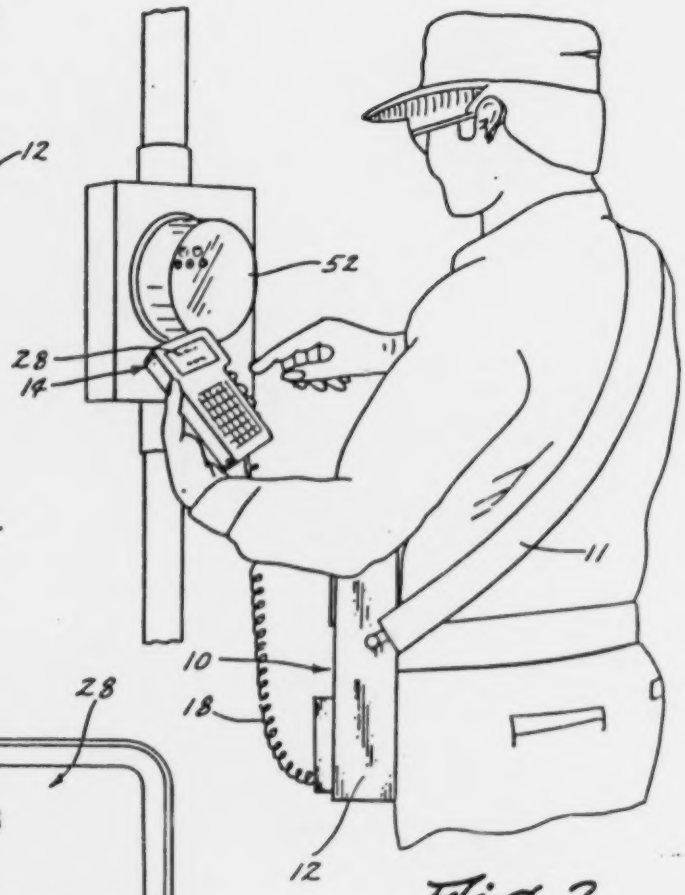


Fig. 2

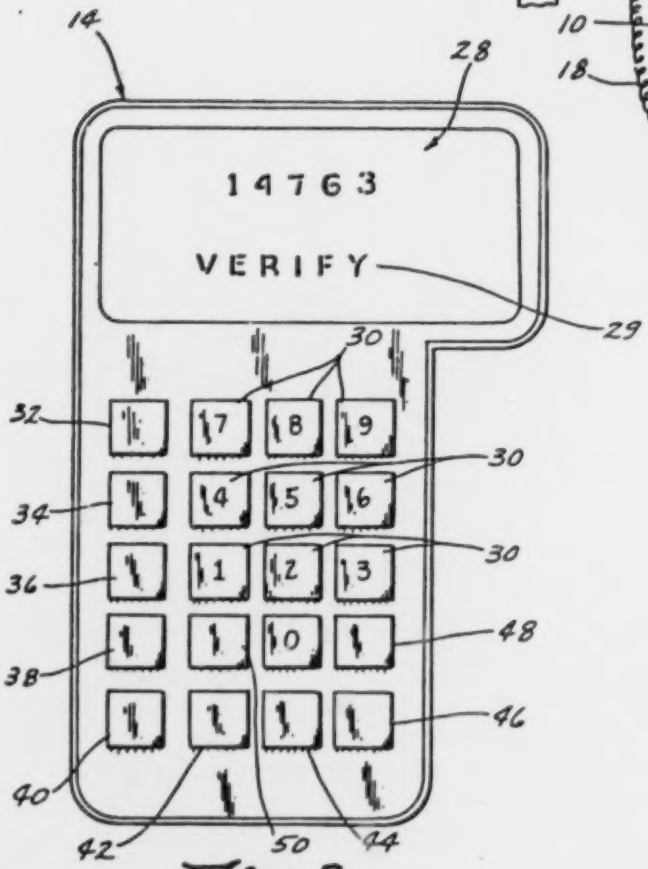


Fig. 3

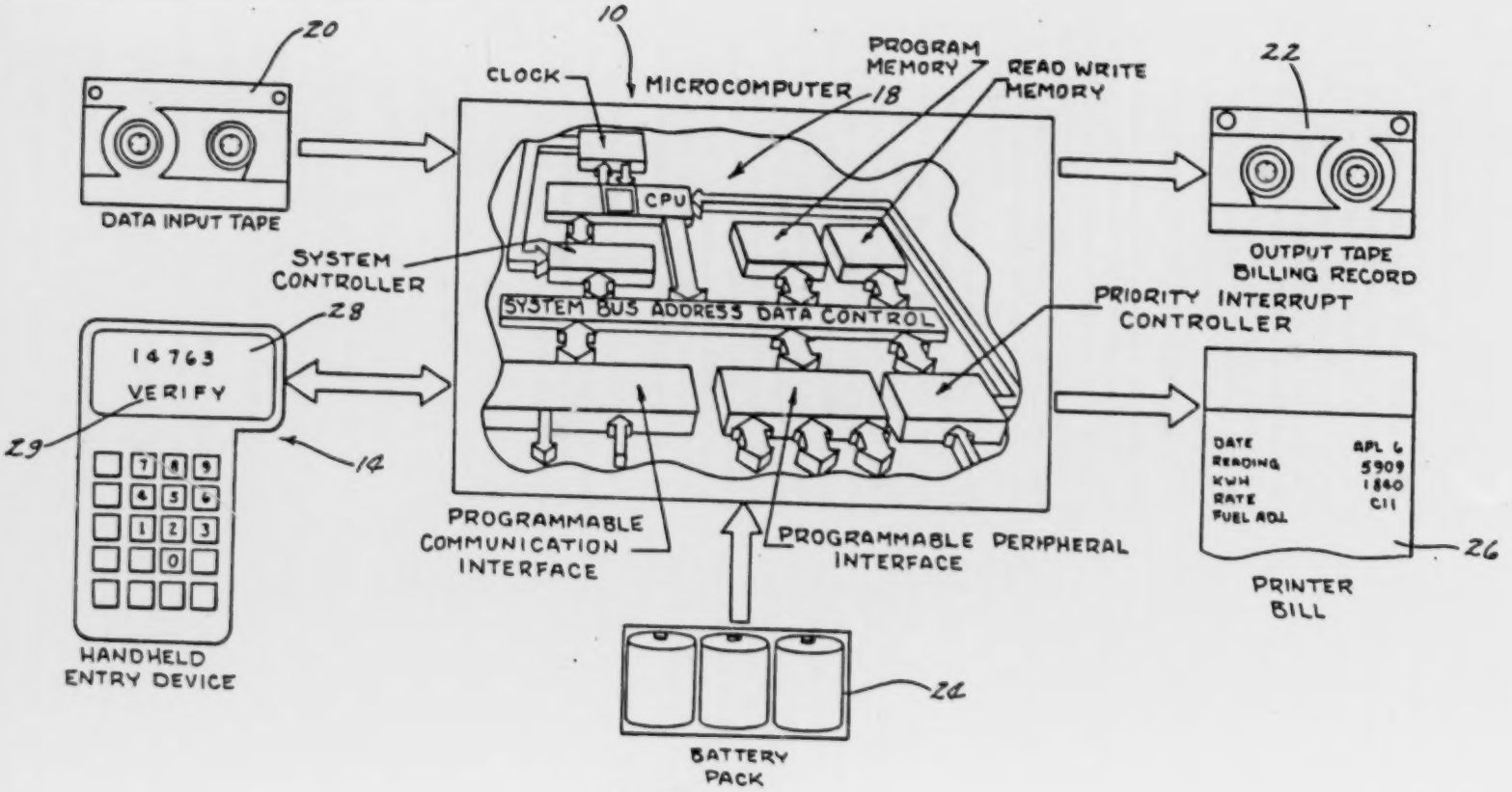

20
10
CLOCK
MICROCOMPUTER
PROGRAM MEMORY
READ WRITE MEMORY
18
22
DATA INPUT TAPE
CPU
SYSTEM CONTROLLER
OUTPUT TAPE BILLING RECORD
SYSTEM BUS ADDRESS DATA CONTROL
PRIORITY INTERRUPT CONTROLLER
28
14763
VERIFY
29
14
DATE APL 6
READING 5909
KWH 1840
RATE C11
FUEL ADJ
26
PROGRAMMABLE COMMUNICATION INTERFACE
PROGRAMMABLE PERIPHERAL INTERFACE
PRINTER BILL
HANDHELD ENTRY DEVICE
24
BATTERY PACK

Fig. 4

054

METHOD AND MEANS OF ASSIMILATING UTILITY METER DATA

BACKGROUND OF THE INVENTION

This invention relates to a method and means for assimilating utility meter data at the meter location. Utility meters are conventionally read at the site of the meter, this information is returned to a central depository wherein the bill for utility usage is computed. The bill is then sent to the customer. This is a very cumbersome means and is quite expensive. The postage alone for this process amounts to hundreds of thousands of dollars for a given utility company. The time lag occasioned by the above process delays the payment of the bills by the customer. Some remote means have been devised so that meters can be read from a central location, but this system requires the installation of special meters which are quite expensive.

SUMMARY OF THE INVENTION

This invention comprises a method and means for assimilating utility meter data at the meter location through the use of a portable computer having both an input tape and output tape. The meter is capable of computing the bill on the spot, and the printed bill is removed from the computer and immediately deposited with the customer.

The input tape includes customer profile information including the customer's name, meter number, account number, service address, and information relating to previous meter readings and debit-credit transactions. The computer device has a handheld control means which includes a visible message output board. The operator through the use of the control means has the ability to recall information to the output board which is stored in the computer wherein the customer's name, meter number, etc. can be visually observed. The current meter information is put into the computer through the control means, the computer calculates the customer's bill, and then prints the bill whereupon it is removed by the operator and deposited with the customer.

This invention eliminates the high cost of mailing bills to the customer and eliminates the time loss occasioned by conventional means wherein the customer does not receive the bill until several days, at best, after the meter is read.

This invention therefore substantially accelerates the rate of payment from meter readings, eliminates postage costs, and greatly facilitates the meter reading record keeping burden.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of the portable computer which comprises a part of this invention;

FIG. 2 is a perspective view of a operator operating the computer of FIG. 1 at the meter site;

FIG. 3 is a plan view of the control means for the computer; and

FIG. 4 is a schematic view showing the manner in which the computer means of FIG. 1 operates.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A small portable computer 10 having a shoulder harness 11 secured thereto has most of its components conventionally mounted within housing 12. A handheld manual control means 14 is connected to the housing 12 by flexible coupling 16.

The computer 10 is comprised essentially of conventional hardware well-known in the art and the precise electronic circuitry is not disclosed herein. With reference to FIG. 4, the numeral 18 designates the computer circuitry. The housing 12 is adapted to receive input cassette tape 20 which is placed in operational contact with the computer circuitry 18 by conventional means. Similarly, output cassette tape 22 is also connected to the computer circuitry 18. A conventional battery pack 24 is mounted within the housing 12 and serves as the energy source for the computer. A printed bill 26 is produced by the computer through conventional means, and the bill 26 is conventionally detachable from the computer.

The control means 14 includes a visible message output board 28 which is comprised of a conventional character display panel such as that disclosed in U.S. Pat. No. 3,868,535 issued Feb. 25, 1975. The numeral 29 indicates a typical message output.

The control means 14 includes a plurality of depressible switches which serve to recall information from the computer for display on the output board 28, and which serve to permit raw data to be placed within the computer. The nine switches 30 are used to place raw data from the utility meter into the computer. The numbers appearing on switches 30 correspond to the value of the data being imposed into the computer from the meter itself.

Switch 32, as will be described hereafter, is the ready switch which is used to institute the process of this invention. Switch 34 actuates the printer of the computer. Switch 36 actuates the read circuitry. Switch 38 designates any peculiar irregularities pertaining to the transaction. Switch 40 is used to verify the reading. Switch 42 is used to determine special codes or instructions. Switch 44 causes the name and address of the customer to be displayed. Switch 46 is the advance switch which will be discussed hereafter. Switches 48 and 50 are special keys to be used for particular circumstances.

A typical electrical utility meter 52 with typical meter dials 54 is shown in FIG. 2.

The input tape 20, sometimes referred to as the route cassette, normally would include the following customer profile information and special instructions:

Customer Profile	Special Instructions
Account number	1. Instruction/codes
Service address	Dog
Meter number	Key in Office
Name	Meter inside
Previous Reading Date	
Previous Reading/Usage	2. Location Codes
Maximum Use	In House
Estimated Maximum Reading	
Rate factors/designation	3. Special Codes
Debit/credit	Tampering
Deposit	
Special Information	

This information is deposited on input tape 20 for a plurality of customers. The operator will pick up the input tape from a central depository before leaving on his route for the day. The tape is placed in the computer in operative connection with the computer circuitry 18.

Upon arriving at the location of the first utility customer, the operator will actuate the ready switch 32 which causes the service address of the customer to be

displayed on board 28. Advance switch 46 will be actuated to cause any special instructions to be imposed on board 28, such as to "beware of a dog", or "see the building manager before reading the meter". Normally, the operator will continue to actuate advance switch 46 until no further information is depicted on board 28. He will continue to actuate the advance switch 42 so that at least the meter location in the house and the meter number will be depicted on board 28.

While standing before the meter as indicated in FIG. 2, the operator will read from the meter, and place the meter reading in the computer by actuating various of the switches 30. The read switch 36 is then actuated to cause the computer to calculate or otherwise take into account the following factors:

Computes the kilowatt hour usage.

Substracts the last month's reading from the new reading.

The utility rate is applied.

Applies debt/credit entries.

Applies any special factors.

By programming the computer with the degree day factors for the prior thirty days, the computer will estimate what the usage should be, based upon prior usage for similar periods. If the usage does not fall within a predetermined range, the operator will be required to reconfirm the current reading before the computer prints the bill. Thus, before the computed bill is printed, the operator will actuate switch 40 to cause the computer to compare the computed bill with the estimated usage. If the computed bill is out of proportion with the estimated bill, the term "verify" will be imposed on the board 28 as indicated in FIG. 3. The operator will then reread the meter and the foregoing steps will be reated.

If the term "verify" does not appear on screen 29, the operator actuates switch 40 to cause the bill 26 to be printed. The operator then removes the bill 26 from the computer. It is deposited in a plastic sack and placed on the door knob of the dwelling involved. As the computer prints the bill, the new billing information is recorded on output tape 22. The switch 44 can be actuated at any time to verify the name and address of the customer. The operator can impose on the output tape irregularities such as broken seals on the meter or the like by actuating switch 38. Similar information such as ross dogs or the like can be imposed on the output tape y switch 42. Keys 48 and 50 are also available for pecial instructions such as indicating that the battery ack is low, the paper supply is low, or the input or utput tapes are low.

At the end of the day, all of the customers on the oute have been billed on the day that their respective eters were read. The output tape is deposited by the perator at a central depository wherein the new information is utilized to create an input tape for the following month. If the meters are being read in a small town, e information from the output tape can be electronilly transmitted through conventional means through central depository in a remote city for processing.

The foregoing invention achieves at least the following objectives:

1. Accurate billings with less chance of mistakes and ay vertification by the customer.

2. Eliminates the necessity of inhouse preparation of e bill.

3. Eliminates the cost of delivering the bill to the stomer.

4. Accelerates utilities' accounts receivable.

It should be understood that the input tape 20 and the output tape 22 are the most convenient means for achieving the respective functions of these components. However, other information storage systems could be utilized in lieu of the cassette tapes without departing from this invention.

It is, therefore, seen that this invention achieves a substantial improvement in the process of assimilating utility meter data.

I claim:

1. A method of assimilating utility meter data at the meter locations, comprising,

accumulating on an input information electronic storage means customer profile information for a plurality of meter customers, said profile information including the customer identity and account information,

placing said input information electronic storage means in a portable computer capable of being manually carried to the site of a given meter, said portable computer having an output information storage means and having the capability of updating, printing and presenting various of said customer profile information for said meter customers before and after receiving current customer profile information,

actuating said computer to segregate and to visually present from the customer profile information for a plurality of meter customers stored on said input information electronic storage means at least the meter number and customer identity information of a given meter customer,

imposing into said computer the current meter reading of said given meter customer at the site of the meter being read,

actuating said computer to calculate the charge for utility usage based upon the previous meter reading and said current meter reading,

actuating said computer to print a bill for said meter customer at the site of said meter based upon said calculation and imposing on said output information storage means the updated customer profile information,

and depositing said bill at the service address of said given meter customer.

2. The method of claim 1 wherein said aforementioned steps are repeated for all of the customers on said input information storage means.

3. The method of claim 1 wherein said customer profile information includes average quantities of utility usage of prior periods, comparing said average quantities of utility usage with the utility usage for the period being read so that substantial variations between the average quantities of utility usage and utility usage determined for the period being read can be ascertained, and signaling the existence of such substantial variations so tha the accuracy of the utility usage for the period being read can be verified.

4. The method of claim 1 wherein the updated customer profile information on said output information storage means is transmitted to a central depository of customer information.

5. A device for assimilating utility meter data at the meter location, comprising,

a portable computer means comprising a computer housing, computer circuitry, input information electronic storage means and output information

electronic storage means operatively connected to said computer circuitry, said input information electronic storage means containing customer profile information for a plurality of meter customers, printout means operatively connected to said computer circuitry,

and manual control means for actuating said computer circuitry and for putting raw data into said computer means, said manual control means including a visible message output board connected to said computer circuitry whereby the operator can visually observe certain of the information contained in said computer as said information is imposed on an output board, said control means including means for segregating and visually presenting on said output board customer profile information for one meter customer from the customer profile information for a plurality of meter customers stored on said input information electronic storage means.

6. The device of claim 5 wherein said control means is a hand-held control manifold connected to said computer housing by an elongated flexible coupling.

7. The device of claim 5 wherein a shoulder harness is secured to said computer housing for carrying the same.

8. The device of claim 6 wherein a shoulder harness is secured to said computer housing for carrying the same.

9. The device of claim 5 wherein said information storage means are tapes.

* * * * *

ted States Patent [19]
rosio

[11] 3,932,730
[45] Jan. 13, 1976

POINT-OF-ACTION BILLING TRANSACTOR

Inventor: Biagio F. Ambrosio, Woodland Hills, Calif.

Assignee: Electronic Memories & Magnetics Corporation, Los Angeles, Calif.

Filed: Sept. 30, 1974

Appl. No.: 510,560

Related U.S. Application Data

Continuation of Ser. No. 356,303, May 2, 1973, abandoned.

U.S. Cl. ..... 235/61.9 R
Int. Cl.[2] G06K 1/00
Field of Search ..... 235/61.6, 61.8, 61.9; 340/172.5, 149, 149 A, 150, 151

References Cited
UNITED STATES PATENTS

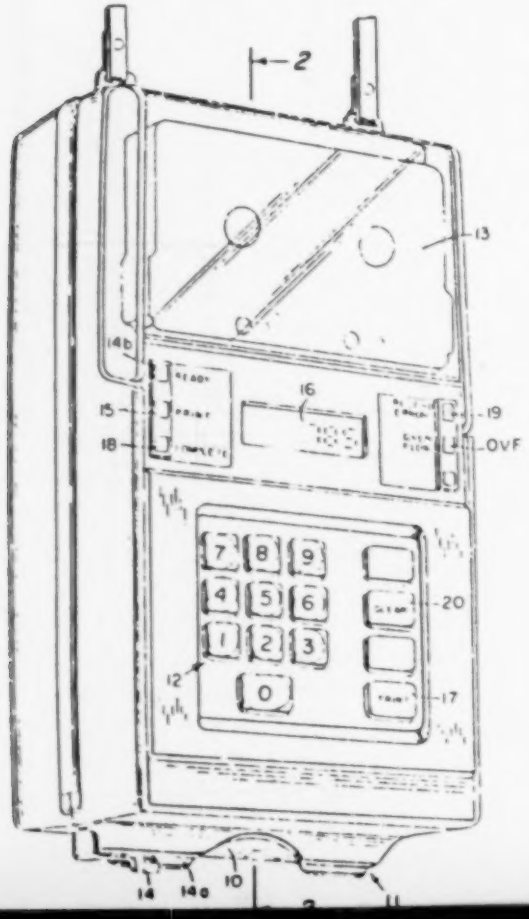
14	4/1969	Simjian	235/61.6
22	2/1970	Perotto et al.	340/172.5
16	4/1970	Affel, Jr. et al.	340/172.5
61	12/1970	Schwarz	235/61.6
20	6/1971	Ishida et al.	235/61.9
52	7/1973	Ruben	235/168
3,770,941	11/1973	Gechele et al.	235/61.7 R

Primary Examiner—Daryl W. Cook
Attorney, Agent, or Firm—Lindenberg, Freilich, Wasserman, Rosen & Fernandez

[57] ABSTRACT

A utility billing transactor is disclosed for entering a new meter reading, computing the amount of utility service delivered as the difference between a previous meter reading and the new meter reading, computing the amount to be paid, and printing a bill showing the new meter reading and the amount due. A card, which has the customer's identification (ID) number, previous meter reading and billing rate code entered on it, is inserted into the transactor to initiate automatic sequencing of steps to: read the ID number, call for keyboard entry of a new meter reading, read the previous meter reading, compute the difference between the meter reading, compute the amount due as the product of a rate or schedule of rates determined from the billing rate code (either directly or through a table stored in a read-only memory) and printing the bill. The entire transaction, including data read from the card and data computed is recorded in nonvolatile memory and immediately checked for recording error.

5 Claims, 11 Drawing Figures



038

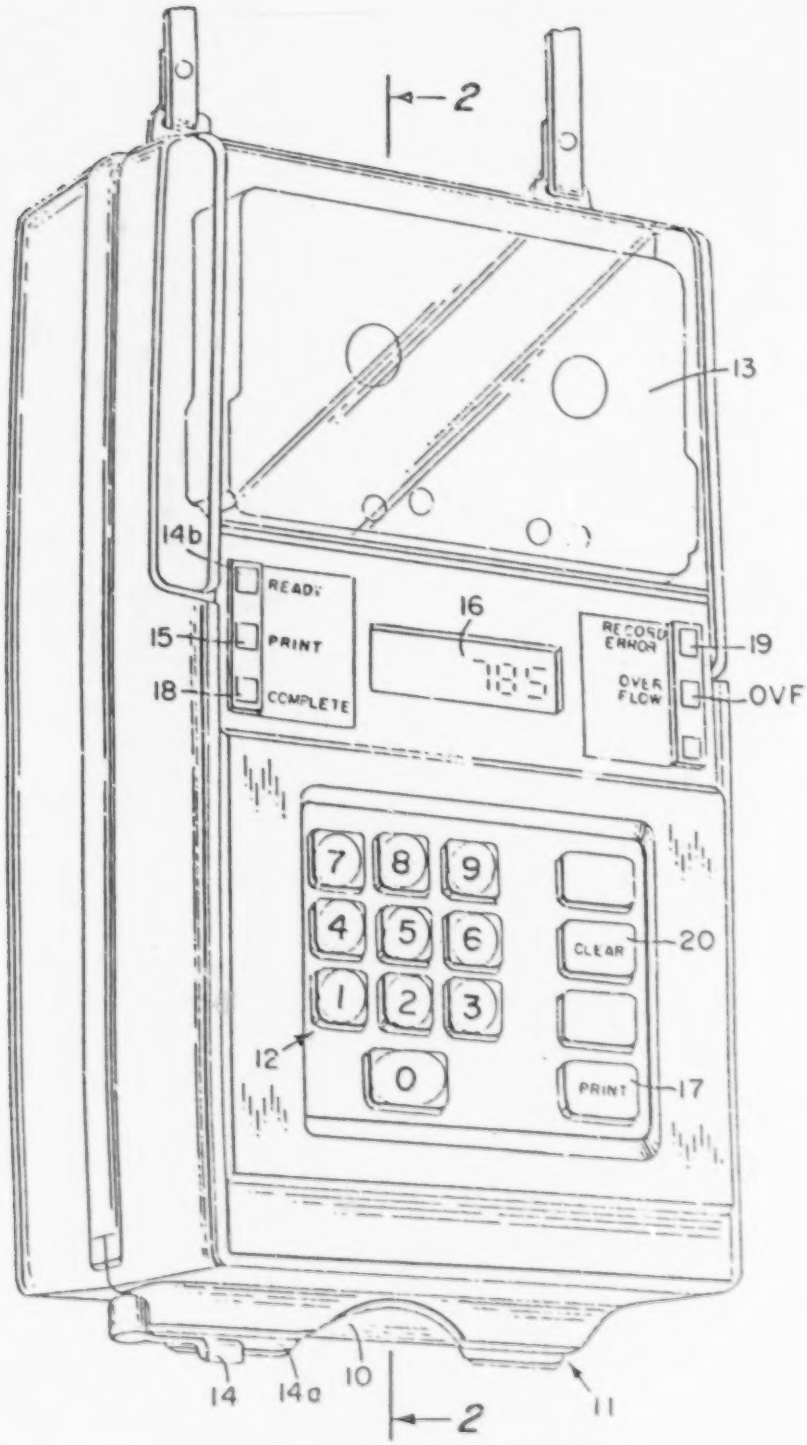

2
13
14b
READ
PRINT
COMPLETE
15
18
16
785
RECORD ERROR
OVER FLOW
19
OVF
7
8
9
4
5
6
1
2
3
0
CLEAR
20
PRINT
17
12
14
14a
10
11
2

FIG. 1

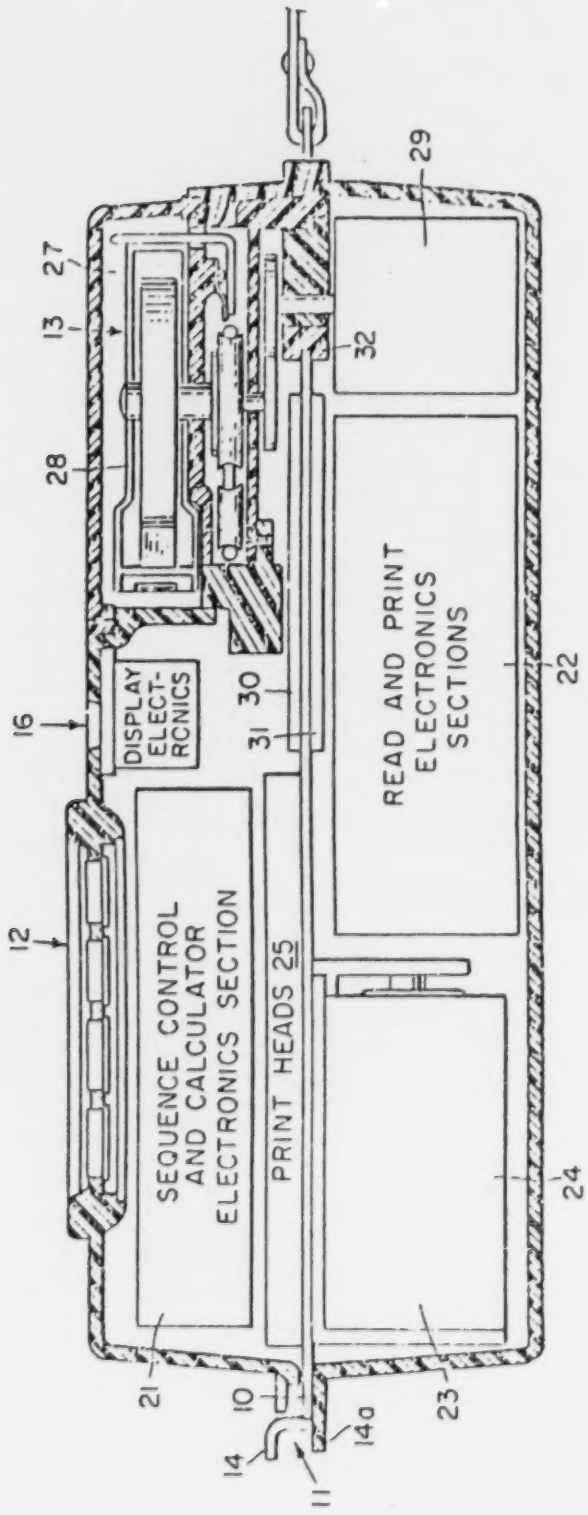

29
27
13
32
28
DISPLAY ELECT-RCNICS
30
31
READ AND PRINT ELECTRONICS SECTIONS
22
16
12
SEQUENCE CONTROL AND CALCULATOR ELECTRONICS SECTION
PRINT HEADS 25
24
21
10
23
14
140
11

FIG. 2

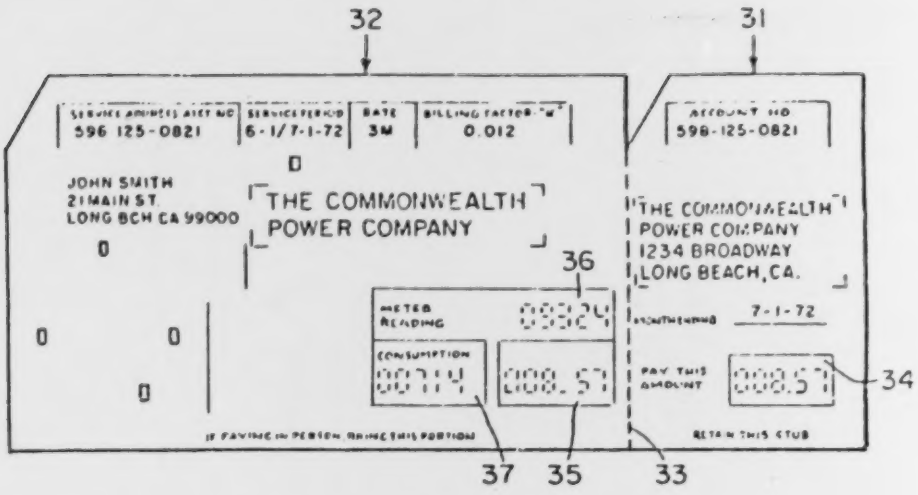

32
31
596 125-0821
6-1/7-1-72
3M
0.012
598-125-0821
JOHN SMITH
21 MAIN ST.
LONG BCH CA 99000
THE COMMONWEALTH
POWER COMPANY
THE COMMONWEALTH
POWER COMPANY
1234 BROADWAY
LONG BEACH, CA.
36
METER READING
08924
7-1-72
CONSUMPTION
00114
008.57
PAY THIS AMOUNT
008.57
34
RETAIN THIS STUB
37
35
33

FIG. 3

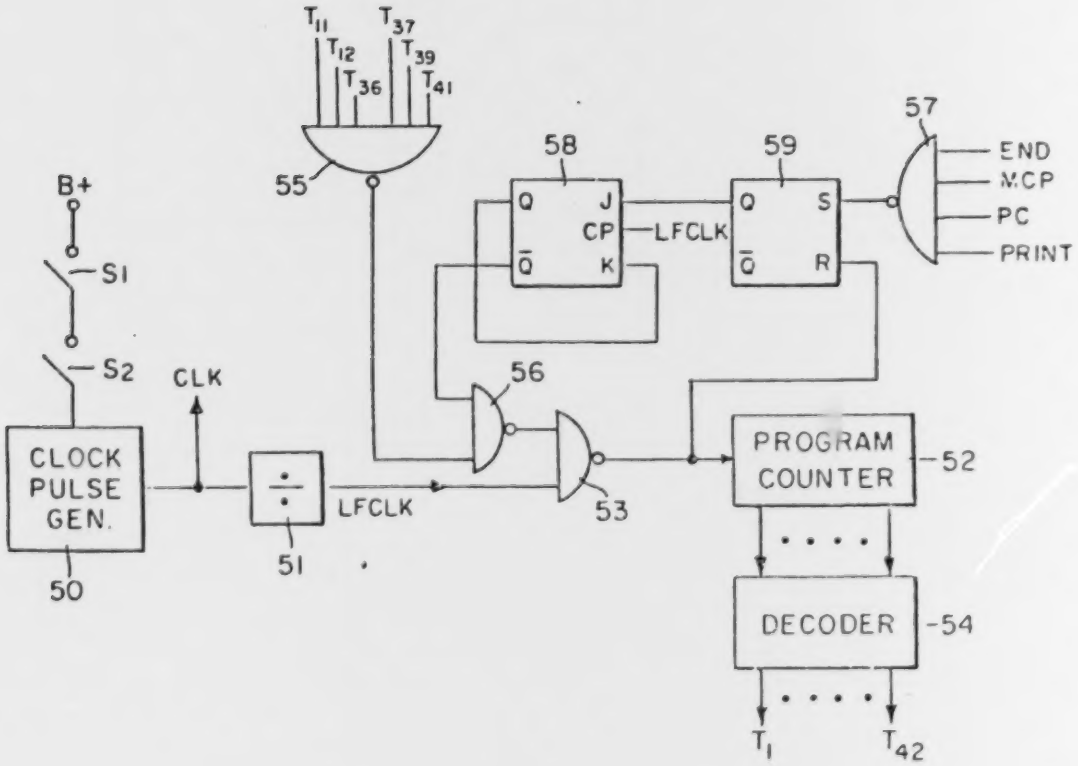
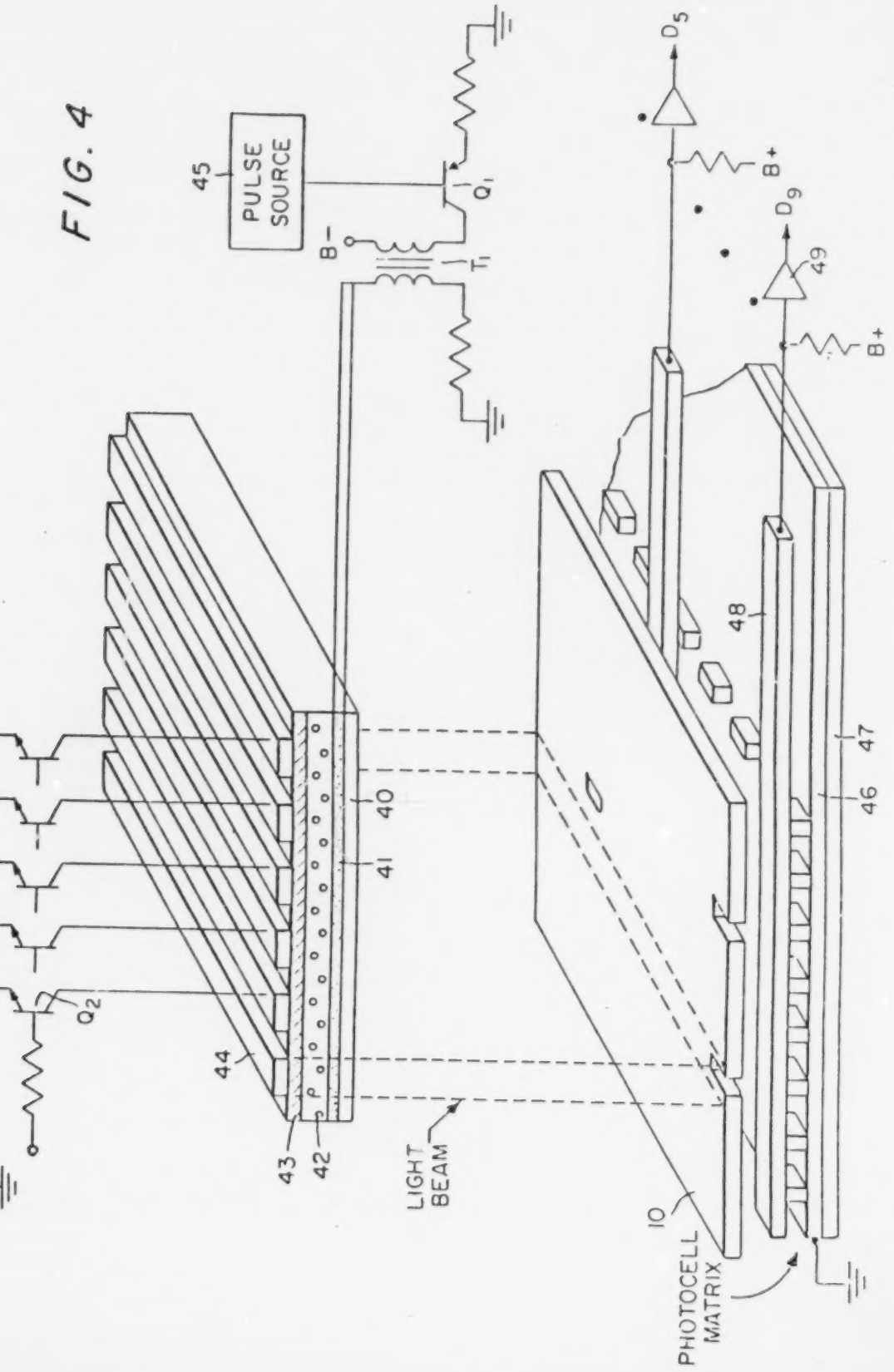

T11
T12
T36
T37
T39
T41
55
58
59
57
Q
J
CP
K
LFCLK
S
R
END
MCP
PC
PRINT
B+
S1
S2
CLK
56
CLOCK PULSE GEN.
50
51
LFCLK
53
PROGRAM COUNTER
52
DECODER
54
T1
T42

FIG. 5

FIG. 4


45
PULSE SOURCE
B-
Q_1
T_1
D_5
B+
D_9
49
B+
48
47
46
40
41
44
43
42
Q_2
LIGHT BEAM
10
PHOTOCELL MATRIX

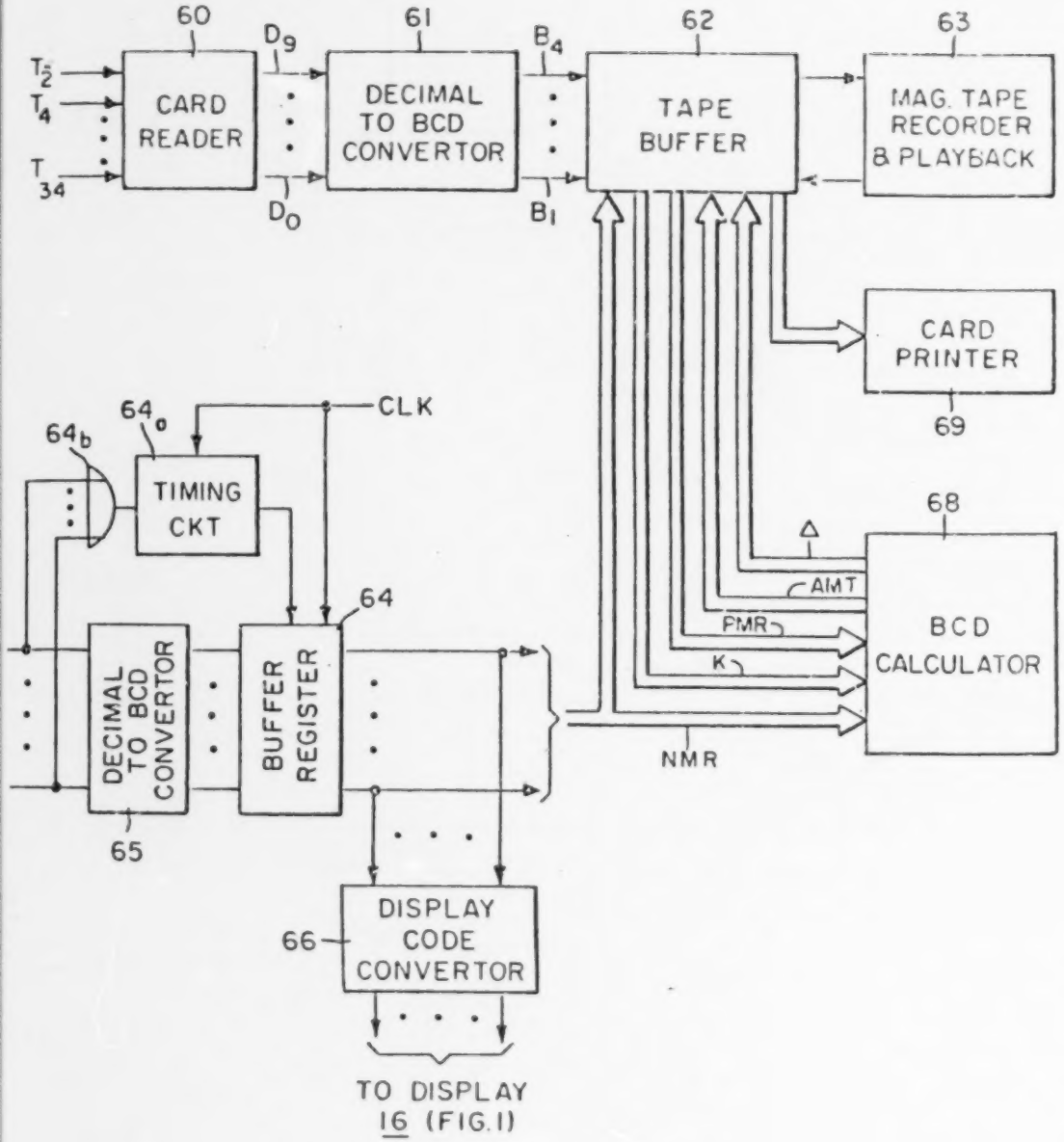

60
CARD READER
T_2
T_4
T_{34}
D_9
D_0
61
DECIMAL TO BCD CONVERTOR
B_4
B_1
62
TAPE BUFFER
63
MAG. TAPE RECORDER & PLAYBACK
CARD PRINTER
69
CLK
64_a
64_b
TIMING CKT
64
BUFFER REGISTER
DECIMAL TO BCD CONVERTOR
65
68
BCD CALCULATOR
AMT
PMR
K
NMR
66
DISPLAY CODE CONVERTOR
TO DISPLAY 16 (FIG. 1)

FIG. 6

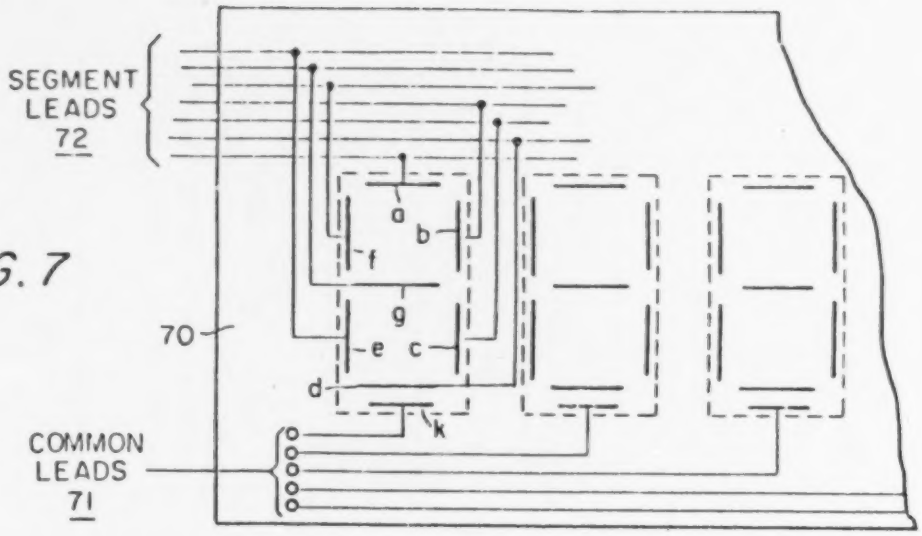

SEGMENT LEADS 72
a
b
f
g
e
c
d
k
70
COMMON LEADS 71

FIG. 7

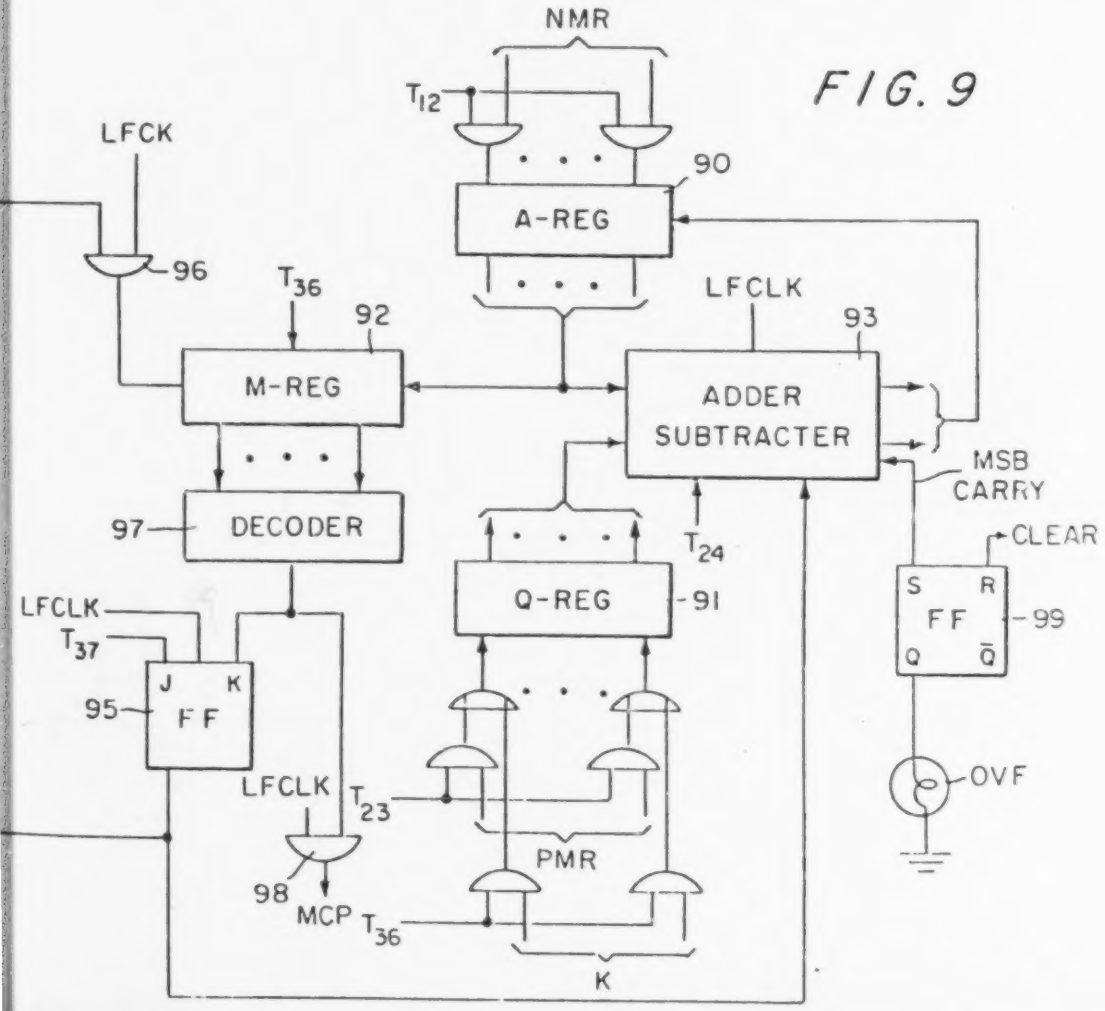

NMR
T12
LFCK
90
A-REG
96
T36
92
LFCLK
93
M-REG
ADDER SUBTRACTER
MSB CARRY
97
DECODER
T24
CLEAR
LFCLK
Q-REG
91
S
R
FF
99
Q
Q̄
T37
J
K
95
FF
OVF
LFCLK
T23
PMR
98
MCP
T36
K

FIG. 9

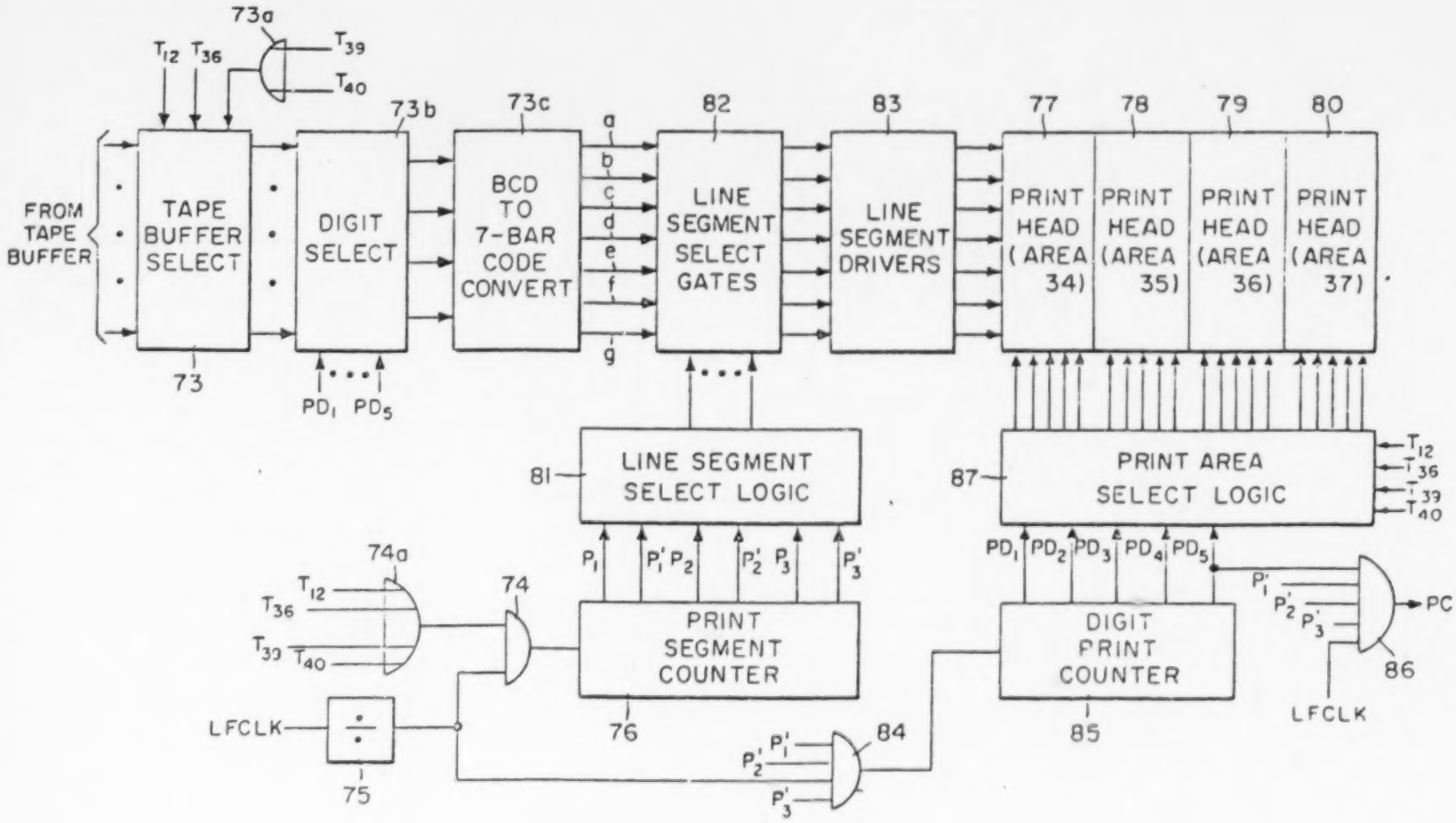

73a
T12 T36
T39
T40
73b
73c
82
83
77
78
79
80
FROM TAPE BUFFER
TAPE BUFFER SELECT
DIGIT SELECT
BCD TO 7-BAR CODE CONVERT
a
b
c
d
e
f
g
LINE SEGMENT SELECT GATES
LINE SEGMENT DRIVERS
PRINT HEAD (AREA 34)
PRINT HEAD (AREA 35)
PRINT HEAD (AREA 36)
PRINT HEAD (AREA 37)
73
PD1 PD5
81
LINE SEGMENT SELECT LOGIC
87
PRINT AREA SELECT LOGIC
T12
T36
T39
T40
P1
P1' P2
P2' P3
P3'
PD1 PD2 PD3 PD4 PD5
74a
74
T12
T36
T39 T40
PRINT SEGMENT COUNTER
DIGIT PRINT COUNTER
P1'
P2'
P3'
PC
86
LFCLK
LFCLK
75
76
84
85
P1'
P2'
P3'

FIG. 8

FIG. 10

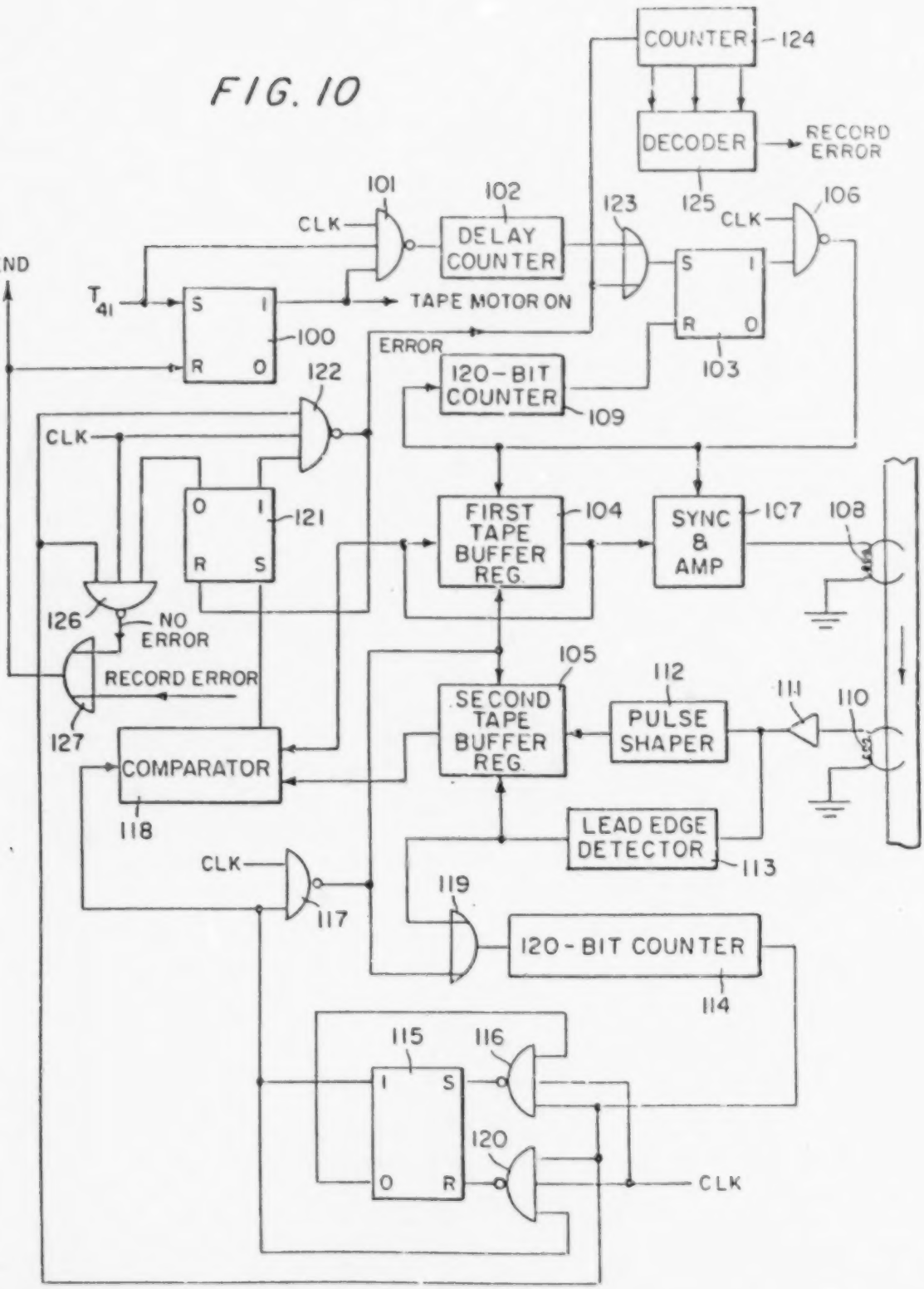
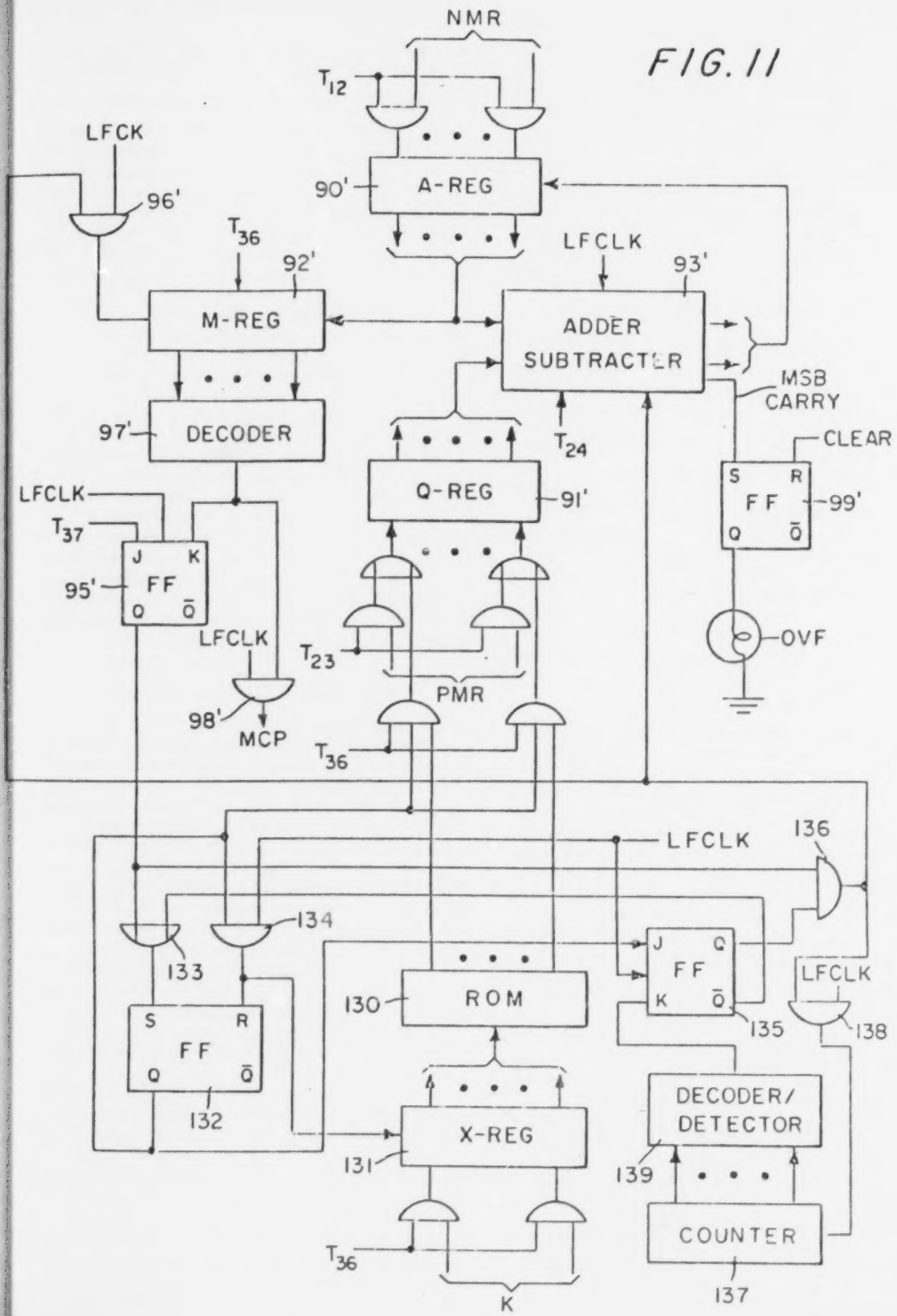

COUNTER
124
DECODER
RECORD ERROR
125
101
102
123
106
CLK
DELAY COUNTER
CLK
ND
T_{41}
S
I
TAPE MOTOR ON
100
R
O
ERROR
103
122
120-BIT COUNTER
109
CLK
O
I
121
FIRST TAPE BUFFER REG
104
SYNC & AMP
107
108
R
S
126
NO ERROR
RECORD ERROR
127
105
112
SECOND TAPE BUFFER REG
PULSE SHAPER
111
110
COMPARATOR
118
LEAD EDGE DETECTOR
113
CLK
119
117
120-BIT COUNTER
114
115
116
I
S
120
O
R
CLK

FIG. 11


NMR
T_{12}
LFCK
96'
90'
A-REG
T_{36}
92'
LFCLK
93'
M-REG
ADDER
SUBTRACTER
MSB
CARRY
97'
DECODER
T_{24}
CLEAR
Q-REG
91'
S R
FF
Q $\bar{Q}$
99'
LFCLK
T_{37}
J K
95'
FF
Q $\bar{Q}$
OVF
LFCLK
T_{23}
PMR
98'
MCP
T_{36}
LFCLK
136
134
133
J Q
FF
K $\bar{Q}$
LFCLK
130
ROM
135
138
S R
FF
Q $\bar{Q}$
132
DECODER/
DETECTOR
X-REG
131
139
COUNTER
T_{36}
137
K

POINT-OF-ACTION BILLING TRANSACTOR

This application is a continuation of application Ser. No. 356,503, filed May 2, 1973, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to apparatus which accepts a record medium prepared with necessary data for billing a utility customer upon reading and entering through a keyboard a new meter reading.

Past efforts to provide a utility-meter reader with portable apparatus for entering a new meter reading and calculating the amount due since the previous meter reading have not been adopted for use by utility companies because of the limited time the meter reader has to cover his route. It would obviously take too much time for the meter reader to plug his portable apparatus into the meter for automatic reading. Consequently, the past efforts have been directed to apparatus into which the meter reader merely keys in the new meter reading, such as shown in U.S. Patent No. 3,590,220. However, that apparatus requires many manual operations to control the sequence of operations, thus burdening the meter reader to the point where he may require more time to complete his route. What is required is a fully automatic billing transactor which responds to the insertion of a previously prepared record medium, such as a billing card, to control the necessary sequence of operations, including the manual entry of a new meter reading, for the amount due to be calculated and for the transaction to be recorded on the record medium for immediate delivery to the customer as a "utility bill."

SUMMARY OF THE INVENTION

The invention is characterized by apparatus having means for accepting a record medium on which there is prerecorded a customers identification number, previous meter reading and a code indicating the rate to be charged the customer for the utility service consumed. The apparatus includes means for reading the data recorded on the record medium. Means for entering the new meter reading through keyboard, means for calculating the difference between the new meter reading and the previous meter reading, means for computing the amount due based upon the difference computed as a function of the applicable rate indicated by the billing rate code, either directly or through addressing a random access memory in which a rate schedule is stored, and printing on the record medium at least the new meter reading and the amount due, all automatically, except for entry of the new meter reading which is automatically called for in proper sequence but is manually entered before the sequence of operations resumes. Sequence control means in the form of prewired logic elements, including a sequence counter, responds to clock pulses once a record medium is inserted into the accepting means to control in sequence the operation of the foregoing means. When entry of the new meter reading is required as the next step, inhibiting means included in the sequence control means inhibits clock pulses from being applied to the sequence control counter until the new meter reading has been entered. The sequence control means also controls printing of at least the new meter reading and the amount due at appropriate times. The computed difference and amount due is printed automatically after the amount due has been computed.

The novel features that are considered characteristic of this invention are set forth with particularity in the appended claims. The invention will best be understood from the following description when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of an exemplary embodiment of the invention.

FIG. 2 is a sectional view taken along the line 2—2 of FIG. 1.

FIG. 3 shows a billing card adapted for use in the exemplary embodiment.

FIG. 4 illustrates in an exploded isometric view an arrangement for a punched card reader in the exemplary embodiment.

FIG. 5 is a logic diagram of a sequence control unit for the exemplary embodiment.

FIG. 6 is a block diagram showing a preferred arrangement for the electronic system of the exemplary embodiment.

FIG. 7 illustrates schematically an arrangement of printing heads for printing on electrosensitive areas of the card in FIG. 3.

FIG. 8 is a logic diagram of a card printer in the system of FIG. 6.

FIG. 9 is a logic diagram of a calculator in the system of FIG. 6.

FIG. 10 is a logic diagram of a magnetic tape recorder in the system of FIG. 6.

FIG. 11 is a logic diagram of an alternative calculator in the system of FIG. 6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows in perspective an illustrative transactor adapted to receive a billing card 10 of a particular utility customer in a slot 11. The card is prepared in advance for the purpose of reading the utility meter and preparing a bill. The necessary information unique to the transaction and required for the new bill is read from the card. The new meter reading is entered through a keyboard 12. The keyboard includes push-button keys numbered 0 through 9 for entering the new transaction with the most significant digit first and a fixed decimal point. As in conventional desk calculators, leading zeroes need not be entered because the digits entered in sequence are shifted serially through the least significant digit position into more significant digit positions. The keyboard includes additional push-button keys to provide what little operator control is required by the transactor over the data processing for the particular transaction.

For simplicity in describing this first exemplary embodiment, all numbers entered into the tape buffer and the calculator are limited to five decimal digits. However, through the technology of integrated circuits, it would be feasible to provide as many as eight or ten decimal digits, and internal registers are provided with sufficient digit capacity to provide the precision desired in the calculations.

Pertinent data involved in the transaction is stored in a nonvolatile bulk store memory 13 for later use by a central office in updating the customer's account, including the total amount to be paid. Some of the data read from the card by the transactor is preprinted on

he card in a form suitable for the customer to read. ransaction data not read from the card by the transac-r, but entered through the keyboard and developed y the transactor, is stored in the bulk store memory nd is printed on the card. The billing card is then eady for immediate delivery to the customer.

It is contemplated that the transactor will be repeat-dly used for the same type of transaction, namely gas, ater or electricity billing, in order that all of the data rocessing may be preprogrammed in such a manner at the required sequence, or sequences, will be pre-ired in a sequence control section. The operator need nly insert the card and secure it in place by pivoting a tch 14 over the slot 11 to hold the card in place. hen a READY light 14*b* comes on, the operator erely enters the new meter reading as transaction atum. When the datum has been entered, a print light comes on and a display window 16 shows the datum ntered. Once satisfied that the datum has been cor-ctly entered, the operator depresses a PRINT button 7, and the transactor will accept the entered datum r automatic processing. When the processing is com-lete, a light 18 comes on. That light remains on until CLEAR button 20 is depressed to clear the transac-r, or until the billing card is removed, at which time e transactor is automatically cleared. The operator vots the latch 14 forward away from a back stop 14a allow the card 10 to be removed. That removes wer from the system, except where necessary, such in a dynamic store memory for preprogrammed quences and/or data tables, if any, by releasing a ing loaded microswitch depressed by the pivotal tch 14 when its position against the stop 14*a*.

Data transferred to the bulk store memory 13 is ecked. If an error occurs in the process of storing the ta, the data is automatically restored until free of ror, or until storing has been attempted a specified mber of times. If successful storing has not been mpleted by then, a record-error light 19 comes on. e operator will then remove the card as usual and rk it "error" for the central office to check or com-te from the new meter printed on the card. If not rrectly printed, the new meter reading can be written the card in pencil.

From the foregoing it is evident that the billing trans-tor shown in FIG. 1 is comprised of five major sec-ns: a keyboard and read section, a sequence control tion, a calculator section, a print section and a bulk re memory section. FIG. 2 illustrates in a cross sec-n along a line 2—2 of FIG. 1 the general layout of se sections. The sequence control and calculator ctronics sections are housed in a compartment 21. e read and print sections are housed in a compart-nt 22. Batteries 23 are housed in a compartment 24. nt heads are housed in a narrow compartment 25 on e side of the card 10 inserted through the slot 11. As l be described more fully hereinafter, each print d is comprised of five 7-bar-segment printing sec-ns capable of numeric line printing of five decimal ls on electrosensitive paper. The bulk store memory oused in a compartment 27. It is comprised of a gnetic tape cassette 28 driven by a motor 29.

he data to be read from the card is stored in the n of punched holes in columns. To sense the ched holes, elongated light emitting phosphorous s are disposed in a thin compartment 30 over the mns to be read, and photocells are disposed under card in a thin compartment 31, one photocell under

each hole position of each column of holes. Slotted guides extending along the sides of the card hold the card in proper position for reading. The latch 14 holds the card secure against a slotted bar 32 extending between the inner ends of the two slotted side guides.

For convenience, electric meter reading and billing will be used by way of example, and not by way of limitation. The billing card shown in FIG. 3 consists of a first portion 31 separated from a second portion 32 by a perforated line 33. The name and address of the utility company is printed on the second portion to be returned with payment, and only the name of the company is printed on the first portion to be retained by the customer for his records. A space 34 is provided for the transactor to enter the amount to be paid in the second portion as well as a space 35 in the first portion. Spaces 36 and 37 are provided for printing the new meter reading entered into the calculator and the consumption (difference between the new meter reading and the previous meter reading) computed by the transactor.

The card is not only a record medium for the bill, it is also a "page" out of the meter reader's route book. On the first portion of each card there is printed essential information from the route book pertaining to the customer, such as the customer's name and address, the customer's account number, the service period, and a billing code or factor, K. The card may also have imprinted thereon by the central office of the utility company a meter identification number, a code indicating the meter location, and the previous meter reading. With this information, the meter reader can carry out his normal function and using the transactor, prepare the bill for immediate delivery at the customer's address.

The first portion of the card has three fields of punched columns: a meter identification field, ID; a previous meter reading field, PMR; and a billing factor or code field, K. These fields are prepunched at the central office. For simplicity in illustrating a specific embodiment of the invention, it is assumed that each field consists of five decimal digits, and that each decimal digit of a value from 0 through 9 is indicated by a punched hole in a corresponding one of ten rows conventionally designated 0 through 9. In practice, a conventional Hollerith card has 80 columns and 12 rows. The top two rows, usually designated 11 and 12, are not used in the first exemplary embodiment to be described, but may be used in other embodiments to provide sequence control over the automatic operation of the transactor.

The account number on the second portion is used at the central office to post the payment. The number can be read optically for sorting. The amount to be paid may also be optically read for posting. If an incorrect amount is received, an opaque overlay can be printed with the amount received. Alternatively, the account number may be prepunched in the second portion for sorting in a field to the left of the space 34. The amount received would then be punched in the remaining columns for automatic posting. In either case, the upper left corner of the returned portion may be precut as a means of checking the proper orientation of that portion in the sorting and posting apparatus.

The upper left corner of the first portion is precut to provide a means of checking proper orientation of the billing card when inserted in the transactor of FIGS. 1 and 2. For example, a microswitch may be mounted

near the bar 32 at the one corner of the card space not intended to receive the cut corner of the card. Inserting the card properly will then close the microswitch and apply power to the transactor. If the cut corner is inadvertently inserted into that corner of the card space, the microswitch will not be closed, thereby forcing the operator to reverse the card in order to proceed. That microswitch is connected in series with the first microswitch referred to hereinbefore, mounted in such a position that it will be closed by the latch 14 only when the latch is in proper latching position against the stop 14a. Thus, the card must not only be inserted properly but also latched in position in order for the power to be applied to the transactor. Removing a processed billing card automatically removes power to conserve the limited power of the batteries.

As will be described more fully hereinafter, the meter reader selects the correct card for a customer and inserts it into the billing transactor. That automatically starts the programmed sequence of the transactor, and preliminary steps are carried out until the new meter reading, NMR, is required. The sequence is then stopped and the READY light is turned on until the meter reader has entered the new meter reading through the keyboard into a keyboard buffer register from which it is displayed in the window 6 using 7-bar segment light emitting diodes for each digit position. The PRINT light then comes on. When the PRINT button is depressed, the new meter reading is stored in a tape-buffer register. It is nondestructively read out from there and printed. It is also entered from there into the calculator section of the transactor.

As will be more apparent from the following description of an exemplary embodiment, all data read from the card is stored in the tape buffer but not all data is printed or is used in the calculator, such as the customer ID number. Data that is to be printed is read from the tape buffer for printing, and data that is to be used in the calculator is transferred to calculator registers.

Once the new meter reading has been entered in the calculator, the previous meter reading, PMR, and the billing rate, K, are read and stored in the tape buffer. Both are entered into the calculater from the tape buffer, and the previous meter reading is printed. Once the consumption (Δ=NMR-PMR) has been calculated, it is also stored in the tape buffer and printed. The amount to be paid is thereafter computed, stored in the tape buffer and printed. For simplicity, in the first embodiment to be described, a constant billing rate or factor is assumed for each customer, although the rate may be different for different classes of customers. It is also assumed that the billing factor includes any applicable tax rate. The amount to be paid is then simply the product of consumption times the billing factor. If the billing factor is not a constant, but decreases in steps as consumption increases, the factor K may be a code used to address a read only memory (ROM) for the applicable rate schedule. The predetermined program for sequencing operations of the calculator would then be expanded accordingly, as will be described for a second embodiment of the invention.

The limit as to what can be included in the bill is only the number of columns on the card, and the extent of transactor memory. In the first embodiment, nothing is to be added to the basic bill so that transactor memory is not required, only the bulk storage unit is provided to store each transaction. If there is a balance due from a previous bill, it can be preprinted on the billing card with instructions to the customer to add that to the amount to be paid for the current billing period.

Once the billing card 10 has been inserted in the slot 11 and the latch 14 is in position to secure the card in place, power is applied to the system, as noted hereinbefore. The first step is to begin reading the card. FIG. 4 illustrates in more detail the card read sections 30 and 31, referred to with reference to FIG. 2. In the light emitting section 30, a thin glass plate 40 is coated with a transparent electrode 41 in a uniform sheet. A film 42 of light emitting phosphor vacuum deposited over the transparent electrode is then coated with a dark dielectric film 43. Metallic electrodes 44 are deposited on the dielectric film in elongated sections over the column positions of cards to be read.

A source of pulses 45, such as a relaxation oscillator, energizes the light emitting film with high negative voltage through a PNP transistor Q_1 and a step-up transformer T_1. However, electrons are injected into the light emitting film only when an elongated electrode 44 is selectively connected to circuit ground, such as by a switch comprised of a transistor Q_2. The phosphor then emits light along the entire length of the selected electrode. That light passes through a hole in the card column positioned below the elongated electrode. A discrete photocell in a matrix detects the light emitted by phosphor.

In the photocell matrix, there is one photocell for each hole position of each column. Therefore, to read 15 columns of 10 rows, there are 150 photocells arrayed in rows and columns. Each photocell is connected between a metallic sheet 46 deposited on an insulating substrate 47 and a separate transparent electrode 48 running across photocells along each row. In that manner, selectively energizing one column electrode 44 illuminates a column of hole positions 0 through 9. Only one hole is punched in a column. Consequently, only one row electrode 48 will conduct, thus indicating the decimal digit stored in the card column illuminated according to the position of the conducting electrode in the array. An amplifier 49 inverts and amplifies the pulse produced.

Referring now to FIG. 5, a clock pulse generator 50 is turned on when microswitches S_1 and S_2 are closed by the proper insertion of a billing card and a proper positioning of the card latching lever 14, as described hereinbefore. The pulse generator may in practice be the same self starting relaxation oscillator used for the card reader as just described. A multivibrator, or other pulse shaping circuit, at the output of the generator provides the proper shape and amplitude for the clock pulses. The nominal frequency of the clock pulses (CLK) thus produced is 250 KHz for use in the system to be discussed with reference to FIG. 6.

A frequency divider 51 reduces the system clock to a lower frequency clock (LFCLK) such as 250 Hz, for use in driving a program counter 52 through a NAND gate 53. A decoder 54 decodes the binary output of the counter and provides timing signals T_1, T_2, T_3 ... T_{42} used in controlling the sequence of operations in the system of FIG. 6. When more than one period of the pulse train derived from the frequency divider 51 is required for the operation called for by a timing signal T_n, the complement T_n' of the timing signal disables the counter through NAND gates 55 and 56. The second input terminal of the gate 56 is true (1) until it is time to release the hold on the counter 52.

nce the operation is complete, a signal indicating
pletion, or otherwise indicating that the program
ence should be advanced to the next step, releases
"hold" imposed on the pulses to the counter
ugh a NAND gate 57 and flip-flops 58 and 59. That
one by setting the flip-flop 58 which enables the
LFCLK pulse to set the flip-flop 59. The first
LK then gated out to the counter 52 then resets the
flop 58. The gates 55 and 57 function as OR gates
e gate 53 functions as an AND gate. The gate 56
provides the inhibit function. The flip-flop 58
onds at its set and reset input terminals to a positive
g step voltage. Consequently, all inputs to the gate
are normally positive (1) to hold the output at a
ative (0) level. When a releasing signal drops one
t terminal to a negative (0) level, it produces a rise
he output terminal of the gate to a positive, thus
ducing a positive going step voltage. Once released,
counter will receive clock pulses and advance the
gram sequence through successive steps until again
bled via gate 55.

he system organization of a card reader-tape store,
board entry and display, calculator and card printer
now be described with reference to FIG. 6. A card
er 60 implemented as described with reference to
4, is energized when the switches S_1 and S_2 are
d, as is the rest of the system, but no column is
inated until time T_2. At time T_1, all system regis-
and flip-flops are reset (cleared) except in the
ence control section of FIG. 5. Then at time T_2,
sistor Q_3 (FIG. 4) is turned on to illuminate column
the card, thus initiating a sequence for reading out
e-digit meter code, $D_5D_4D_3D_2D_1$, from columns
A converter 61 converts each decimal digit signal
4-bit code, B_1–B_4.

time T_3, the most significant digit (MSD) D_5 of the
r ID code read from column 1 is stored in parallel
e MSD position of a thirty-digit (120-bit) register
tape buffer register 62. The next four digits of the
r code are then read in sequence and stored. The
ence is as follows:

- energize Column 1
- store D_5
- energize Column 2
- store D_4
- energize Column 3
- store D_3
- energize Column 4
- store D_2
- energize Column 5
- store D_1

e tape buffer register 62 consists of two shift regis-
as will be described more fully hereinafter with
ence to FIG. 9, each having 120-bit positions for
g six numbers, each having five digits in BCD
Each number is stored in the same manner as the
ode, starting with the most significant digit, with
successive BCD digit being stored in the first
er in the next least significant 4-bit positions.

e first register of the tape buffer register 62 is
led with gates for selectively reading out the five
numbers, in parallel by BCD bits, and in serial or
el by BCD digit as needed. It is also provided with
for recirculating the entire content of its 120-bit
ons for writing into one track of magnetic tape 63
ics by BCD digit and BCD bit without any loss of
The second register is used to store a playback of
corded sequence of 120-bits for comparison with
the content of the first register in order to confirm correct storage of data on the tape. In the event of a detected error, the system will again record on the tape and check the recorded data. Sequence control for that record and check operation occurs at the end of the predetermined program and will be described hereinafter with reference to FIG. 9.

At time T_{11}, when the least significant digit of the ID code is stored in the tape buffer, the program counter is disabled via gates 55 and 56 of FIG. 5. The timing signal T_{11} will also energize the ready light 14 (FIG. 1). The meter reader then knows that the transactor has power and is functioning. He also knows it is time to enter the new meter reading, NMR, by punching the proper keys of the keyboard 12. The keys only enter the digits of the NMR into a buffer register 64 via a decimal to BCD converter 65 with the MSD first in the least significant digit (LSD) position. Each subsequent digit entered shift digits already entered to the left using the leading edge of each keyed digit signal to trigger a timing circuit 64*a* via an OR gate 64*b* to enable the buffer register to shift in response to five fast clock pulses from the generator 50. In practice, the timing circuit will be comprised of a counter which will meter precisely five shift pulses, i.e., which will count five clock pulses and then reset. In that manner the digits entered in the LSD position are shifted in, the direction of the MSD of the buffer register 64 and leading zeroes need not be keyed in.

For simplicity, it is assumed all digits are displayed continuously through a five-digit code converter 66, but in practice the digits may be displayed serially in repeated cycles, thus time sharing a one-digit code converter. Persistence of vision will provide a steady display if the display cycle is repeated every tenth of a second.

Once the meter reader is satisfied he has entered the meter reading properly, he presses the PRINT button to momentarily generate a PRINT signal which sets the flip-flop 58 via the NAND gate 57 in FIG. 5, thereby unlocking the program counter 52. That enables the counter to advance, but at the next count, a signal T_{12}' again disables the program counter. That signal also transfers the content of the buffer register 64 (five BCD digits) into the next five BCD digit positions of the first shift register in the tape buffer. That is instantaneous. In addition, signal T_{12} enters the new meter reading (NMR) into a register (A) in the calculator 68. The program counter is locked at time T_{12} to permit the slow process of printing the NMR out of the tape buffer onto the card.

The card printer 69 to be described with reference to FIGS. 7 and 8 employs non impact, electroprint heads. Each head is capable of printing five digits in a line, each digit is composed of seven bar segments. For convience, only three 7-bar-segment printing sections are shown and connections are shown complete for only the first, it being understood that other printing sections are similarly connected for each digit position of a printing head. The billing card is sensitized for electroprinting each digit with a coating of ZnO on a conductive (carbon) film.

The head illustrated schematically in FIG. 7 consists of a ceramic substrate 70 with seven metallic segments, a through g, for each digit. An eighth "segment" k is provided for making a connection to the common conductive film on the card for the printing of a digit. The common conductive film for each digit is indicated by

a dotted line outlining the area of the print head which is in contact with the digit printing area on the card which carries the conductive film. Common leads 71 are employed to select the digit positions for printing in sequence, while segment leads 72 are employed to select the segments *a* through *g* to be sequentially energized for each digit printed. An alternative arrangement would be to have a conductive film common to all digit positions, and separate logic for selectively energizing the 7-bar segments of each individual digit in sequence. In either case, the current through selected segments and the metallic film darkens the ZnO film and thus prints only in the areas covered by the selected segments.

Referring now to the card printer control logic shown in FIG. 8, a tape buffer select unit 73 in the printer responds to the sequence timing signal T_{12} to select for printing the five BCD digit positions (20-bit positions) of the tape buffer into which the new meter reading (NMR) is entered. The sequence timing signal T_{12} also enables AND gate 74 via an OR gate 74*a* to transmit low frequency clock pulses from a frequency divider 75 to a print segment counter 76. The frequency divider 75 reduces the low frequency clock, LFCLK, to a sufficiently low frequency, such as 25 Hz, to permit printing through a selected electroprint head from a group of heads 77, 78, 79 and 80 for the respective areas 34, 35, 36 and 37 shown on a card in FIG. 3.

The print segment counter 76 is a 3-bit binary counter, the output of which is decoded by line segment select decoder 81 to sequentially gate through a bank of AND gates 82 line segment signals to segment leads of the print heads via line segment drivers 83. The line segment select decoder is simply a logic network for converting the binary output of the counter 76 into a decimal code where only one of seven lines is energized for each of the binary counts from 001 through 111.

After the last segment *g* of the first digit has been selected for printing, if necessary, and the counter 76 cycles to the zero state, an AND gate 84 is enabled to transmit a clock pulse from the frequency divider 75 to a digit print counter 85 implemented as a ring counter having five stages, the first of which is on when the counter is in the reset state in order that a signal PD_1 be transmitted to select the first of five digits to be printed through the first one of five common leads 71 (FIG. 7). In that manner, the first digit is printed before the AND gate 84 transmits a clock pulse to advance the digit print counter to its second state during which a signal PD_2 is transmitted to select the second digit. The sequence is repeated until all five digits have been printed.

A digit select network 73*b* responds to the signals PD_1 through PD_5 to sequentially gate the BCD digits to a BCD to 7-bar code converter 73*c*. In that manner the tape buffer select unit 73 couples a selected group of 5 BCD digits to the digit select network which transmits the four bits of a selected digit to the code converter for printing.

After the fifth digit has been printed and the print segment counter 76 overflows, i.e., returns to the zero state, the next low frequency clock is transmitted through an AND gate 85 as a print complete signal, PC, to the NAND gate 57 in FIG. 6 to unlock the program counter.

The output terminals PD_1 through PD_5 of the print digit counter 85 are connected to a print area select

logic network 87 which permits the print digit counter to energize in sequence the common leads 71 (FIG. 7) of the print head for the area 36 (FIG. 3) in response to the timing signal T_{32}. At time T_{36} when the consumption (Δ= NMR-PMR) is to be printed, the signals PD_1 through PD_5 are effective to select for printing digits through the print head for the area 37 (FIG. 3). That is accomplished through one bank of AND gates enabled by the signal T_{36} to transmit the signals PD_1 through PD_5 to successive ones of the common lines 71 (FIG. 7) for the head of the area 37. Timing signals T_{38} and T_{40} are similarly effective in causing the amount to be paid in areas 34 and 35.

Once printing of the new meter reading is complete and the program counter 52 advances to the count of T_{13} at the output of the decoder 54, a sequence is initiated for reading from the card the previous meter reading, PMR. The sequence is carried out during the timing periods T_{13} through T_{22} where the odd timing periods are used to sequentially illuminate columns 6–10 of the card and the even timing periods T_{14} through T_{22} are used to store the decimal digits read and converted to a BCD code into the five BCD digit positions (20-bit positions) of the first register in the tape buffer.

The PMR read from columns 6–10 of the card is not printed on the billing card by the transactor. If the PMR is to be printed in that portion to be retained by the customer for the customer's information, it may be printed on the card at the time that it is punched into columns 6–10. Consequently, during the next sequence timing period T_{23} the calculator 68 enters the PMR in a register (Q) in parallel. This is possible by having the appropriate 20-bit positions of the tape buffer connected to input terminals of a designated register in the calculator for parallel entry in response to the timing signal T_{23}.

The next timing signal T_{24} commands the calculator to subtract the PMR in the Q-register of the calculator, from the new meter reading, NMR, in the A-register of the calculator, and to store the difference, Δ, in the A-register. The next timing signal T_{25} causes the difference, Δ, to be copied in parallel into the next five BCD digit positions (20-bit positions) of the first register in the tape buffer, without destroying the difference in the A-register in order that it may be multiplied by the billing factor. That is accomplished by simply copying the content of the A-register at that time directly into predetermined positions of the tape buffer register through prewired gates.

The next timing signal T_{26} initiates reading out the billing factor from the card into the tape buffer. That is accomplished during the successive timing periods T_{26}-T_{35}. During successive even periods columns 11–15 of the billing card are sequentially illuminated and during the odd timing periods, the successive BCD digits are entered into successive BCD digit positions (4-bit positions) of the first register in the tape buffer. The next timing signal T_{36} disables the program counter via the gates 55 and 56 and causes the billing factor, K, to be transferred in parallel from the appropriate bit positions of the first register in the tape buffer to a third Q register of the calculator.

The timing signal T_{38} is also applied to the tape buffer select unit 73 and print area select unit 86 to print the difference, Δ, in the area 37 of the billing card before the amount to be paid is computed. That is accomplished in the same manner in which the new meter reading was printed in the area 36 of the billing card.

action is started by the print segment counter 76 in
nse to the timing signal T_{36} applied to the AND
74 via OR gate 74*a*. When printing is complete, a
l PC unlocks the program counter via the NAND
57 as before.

should be noted that for simplicity, it is assumed
all five digits are printed, including the leading
s, but in practice, additional logic may be pro-
d for suppressing the leading zeroes and initiating
ctual printing process with the most significant
zero digit. During this period of suppressing lead-
eroes, the timing sequence of the printer could be
lerated to save time, but the time to be saved
d not normally justify the additional complexity of
control logic. However, it would still be advanta-
s to suppress the actual printing of leading zeroes
der to save the power that would be wasted in
ing such leading zeroes.

should also be noted that the time in the pro-
med sequence during which the difference is
ed is not important. It could just as easily have
printed before reading out the billing factor, K, or
ted until after the amount to be paid is computed
then printed, either before or after the amount to
id is printed.

e next timing signal T_{35} initiates a multiply com-
d in the calculator to cause the difference in the
gister to be multiplied by the rate factor in the
gister through successive parallel additions of the
ence a number of times as designated by the bill-
actor, and storing the partial products. To assure
ient time for this multiplication, the timing signal
isables the program counter. When the multiplica-
s complete, the calculator generates a multiplica-
complete signal, MCP, to unlock the program
er through the NAND gate 57.

ere are many known ways of implementing the
plication process. For simplicity, it is here con-
lated that a third register, which may be referred
the M-register, is provided in the calculator and
emented as a counter which counts down one for
addition step of the multiplication. The first step
multiplication process is to transfer the consump-
Δ, into the M-register at time T_{36}. The M-register
s the content of the Q-register to be added to the
ent of the A-register one time each time it counts
one, thus building up the product in the A-regis-
An advantage of this technique is that in the case of
ple billing factors to be applied according to a rate
lule, such as one billing factor for the first 40
, another for the next KWH, etc., it would be
e to stop the multiplication at the proper time and
another billing rate.

e next timing signal T_{36} initiates a parallel transfer
oduct of the multiplication, i.e., the amount to be
AMT, from the A-register to the next five digit
ons of the first register in the tape buffer. The
fer is in parallel through prewired gates enabled by
ming signal T_{36}.

e next timing signal T_{39} disables the program
ter and initiates printing on the billing card the
nt to be paid from the tape buffer. Because of the
nt of power required to print each segment of a
on the billing card, and the limited power pro-
by the batteries in this portable transactor, the
nt to be paid is first printed in the area 35 of the
g code. The signal T_{39} selects the five digit print
for the area 35 while the signal T_{39} directs the tape

buffer select unit 73 through an OR gate 73*a* to print the amount to be paid in the same manner as the new meter reading, NMR, printed in the area 36 and the difference, Δ, printed in the area 37 labled "consumption".

After the print sequence is complete, a signal PC generated by the print control unit unlocks the program counter which then advances to the next count T_{40} and again locks for another printing cycle, this time to print the amount to be paid in the area 34 through the print head for the area 34 selected by the signal T_{34} while the amount to be paid is again selected by the tape buffer select unit 73 (FIG. 8) as directed by the signal T_{40} through the OR gate 73*a*.

Each time the amount to be paid is printed the printing sequence is commenced when the print segment counter 76 is enabled to receive clock pulses through the AND gate 74 by the timing signals T_{36} and T_{40} via the OR gate 74*a*. Although not shown, it is understood that the print segment counter and print digit counter are reset by the print complete signal even though those counters have by design recycled to their reset state in order to assure that the next printing sequence does start with those counters in their reset state.

When the amount to be paid has been printed the second time, the print complete signal, PC, unlocks the program counter, and the next timing signal, T_{41}, relocks the timing counter via the NAND gates 55 and 56. The signal T_{41} also initiates transfer of the data stored in the first register of the tape buffer into the magnetic tape.

From the foregoing it is evident that in this first embodiment, a fixed program is provided by the program counter. The same organization can be used in other embodiments where the sequence of operations is controlled by stored operation codes read from the billing card, or read from a random access memory as in a conventional programmed digital computer.

The organization of the calculator will now be described with reference to FIG. 9. It is essentially the organization of a conventional arithmetic unit in a programmed digital computer. It contains an A-register 90 used as an accumulator during all arithmetic operations, a Q-register 91, an M-register 92 and a parallel adder/subtracter unit 93. When the previous meter reading in the Q-register is subtracted from the new meter reading at time T_{24}, subtraction logic is enabled in the unit 93. The difference, Δ, is stored in the A-register. At time T_{26}, when the billing factor K is entered into the Q-register, the content (Δ) of the A-register is transferred to the M-register 94 for use as a multiplier during multiplication. The product is developed in the A-register.

In the case of electricity, a typical rate factor may be 5.525 cents per kilowatt hour. Therefore, the multiplication called for would be, for example, 175KWH × 0.05525. The multiplication carried out during time T_{35} is initiated by setting a JK flip-flop 95 to repeatedly add the contents of the A and Q-registers, and to store the sum of each addition in the A-register. Each addition occurs in response to a low frequency clock, LFCLK, which is counted down in the M-register through a gate 96. When the M-register has counted down to one, a decoder 97 detects this condition and enables the next clock, LFCLK, to reset the flip flop 95. The product is then in the A-register. A gate 98 also transmits a clock pulse as a multiplication complete signal, MCP, to the NAND gate 57 (FIG. 2).

The A register and addition logic is sufficiently long to accommodate the largest product anticipated without overflow. Should an overflow (array) from the MSB position of the addition logic, a flip-flop 99 will be set by the MSB carry signal to energize an overflow lamp OVF until the transactor is cleared and the flip-flop 99 is reset. Parallel addition is contemplated in this exemplary embodiment for simplicity. However, in practice it may be desirable to perform addition and subtraction in series by BCD digit and in parallel by binary digits of each decimal digit. The fast clock, CLK, could be used to sequence the successive steps of each serial addition or subtraction.

The product formed in the A-register is with a fixed decimal point. In this exemplary embodiment, the decimal point would be five BCD places from the right. Upon printing out the product as the amount to be paid, only two decimal places to the right of the decimal point are printed. The balance, which is a fraction of one cent, is ignored. If desired, logic could be included to round off at the time of printing.

FIG. 10 illustrates the control logic for recording on tape. The timing signal T_{41} sets a flip-flop 100 to turn the tape motor on, and enables a NAND gate 101 to transmit clock pulses, CLK, to a delay counter 102. The purpose of that counter is to delay transfer of data to the tape until the tape is up to speed. At the end of the delay period, a flip-flop 103 is set to start recording on tape the content of the first register in the tape buffer unit. The first and second registers in the tape buffer unit are shown as two 120-bit registers 104 and 105.

The flip-flop 103 enables a NAND gate 106 to transmit system clock pulses, CLK, to the shift register 104 and to a synchronizing and amplifying unit 107 for storing each binary digit shifted out of the first tape buffer register on tape. The data is preferably shifted out in the order stored in the register with the most significant bit of the MSD of the meter ID first.

A bit zero is stored on the tape as a short pulse less than half the period of a clock pulse (about one-fourth), and a bit one is stored as a longer pulse more than half the period of a clock pulse (about three-fourths) through a write head 108. A counter 107 counts the clock pulses applied to the register 104. When 120 clock pulses have been counted, the counter 109 resets the flip-flop 103 to complete recording one time.

A read head 110 positioned downstream from the write head senses the pulses recorded through the head 108. An amplifier 111 and pulse shaper 112 restores the pulses read to substantially the shape of pulses at the output of the amplifier 107. A detector 113 detects the leading edge of each recorded bit from the amplifier 111 to produce a sharp self-synchronizing pulse and delays it half the period of the clock pulses in order to effectively strobe the output of the amplifier 111 at the center of each bit period. To accomplish that, the delayed pulse is applied to the shift register. If a short pulse is present at the output of the amplifier, indicating a bit 0 read, the pulse from the detector 113 shifts a bit 0 into the register 105. If a long pulse is present at the output of the amplifier, indicating a bit 1 read, the pulse from the detector 113 shifts a bit 1 into the register 105.

Other self-synchronizing record and playback systems may be used, such as simply recording the clock pulses in second channel in parallel with binary digits recorded, using side-by-side write heads. The clock pulses may then be read in a second read head beside the read head 110. However, this or an equivalent self-synchronizing record and playback system is preferred to avoid doubling the number of read heads and having to maintain precise spacing between heads of each pair.

A second 120-bit counter 114 counts the self-synchronizing clock pulses out of the detector 113 to determine when playback of the recorded data is complete. When complete, a flip-flop 115 is set via a NAND gate 116 to enable a NAND gate 117 to transmit system clock pulses to both shift registers 104 and 105, thereby shifting both through a comparator 118. When 120-bits have been shifted through the comparator by clock pulses counted by the counter 114 via an OR gate 119, the flip-flop 115 is reset via a NAND gate 120. The comparator is also enabled by the flip-flop 115.

The comparator is comprised of an exclusive OR gate which indicates an error if its output is ever true while the paired bits are being shifted through it from the two registers. If so, a flip-flop 121 is set. At the end of the 120-bit compare period determined by the counter 114, and while the flip-flop 115 is being reset, the flip-flop 103 is set, via a NAND gate 122 and an OR gate 123, to initiate another recording and playback cycle. At the same time the flip-flop 121 is reset and a counter 124 is incremented to a count of one. If an error occurs again during the second or third time, the counter 124 is incremented each time. If incremented to a count of three, a decoder 125 detects the count and signals RECORD ERROR to turn on the "record error" lamp 19 (FIG. 1). The meter reader may manually clear the error signal by pushing the clear button, but that is not necessary because the transactor clears itself automatically at time T_1 of a new sequence for the next billing card. After pulling out the billing card just processed with an error in recording, he manually fills out a duplicate billing card to return to the central office for checking at the central office, and proceeds to deliver the billing card just pulled out.

If no error occurs during the first, second or third recording cycle, NAND gate 126 signals NO ERROR. That signal, or the ERROR signal, unlocks the program counter via OR gate 127 (FIG. 9) and NAND gate 55 (FIG. 5). The next timing signal T_{42} then turns on the complete lamp 18 (FIG. 1). Upon removing the billing card, the complete lamp is turned off as all power is removed from the billing transactor.

In the foregoing description of a first exemplary embodiment, a constant billing factor was assumed for all of the consumption of a customer. That is often not the case, as will now be described for a second embodiment of the invention with reference to FIG. 11. Instead, a typical monthly bill for electricity may be computed in accordance with the following charges:

First 40 KWH	at 5.525 cents per KWH
Next 40 KWH	at 4.025 cents per KWH
Next 140 KWH	at 2.525 cents per KWH
Next 768 KWH	at 2.025 cents per KWH
Additional KWH	at 1.025 cents per KWH

To accommodate such a rate structure, which may be different for different classes of customers, the rate factor, K, is not entered into the Q-register of the calculator for computing the bill. Instead, the number K is used as a code to address a readonly memory (ROM)

0 where the applicable rate schedule is stored Consequently, at time T_{39}, the number K is stored in an register 131.

In the modified calculator shown in FIG. 11, the mponents common to the first embodiment are idented by the same reference numeral, but distinguished a prime for each reference numeral

The number in the X-register points to a block of cessive memory locations which contain the rates to applied to successive increments of consumed elecal power. Consequently, when the timing signal T_{39} s the flip-flop 95' to initiate multiplication, a flip-p 132 is set via an OR gate 133 to enable the rate to read out from the location in the ROM specified by X-register in response to the next low frequency ck which also resets the flip-flop 132 via an AND e 134 and increments the X-register to the address the next rate That same clock pulse, LFCLK, sets a flip-flop 135 to enable an AND gate 136, and reby enable the adder-subtracter to respond to subquent low frequency clock pulses, LFCLK, for multication by successive addition of the first rate factor m the ROM to the content of the A-register, which ority times for the first 40 kilowatt hours, unless the register 94' which counts the number of additions counted down to one, in which case the decoder causes the flip-flop 95' to be reset with the next ck, LFCLK, to stop the multiplication after the next dition

Assuming the M-register has not counted down to e, multiplication by addition continues with a new e for the next 40 kilowatt hours A counter 137 unts up the number of additions by counting the low quency clock pulses, LFCLK, via a gate 138. When number 39 stored with the rate of 5.524 cents per WH and read from the ROM is detected by a decoder/detector 139, the flip-flop 135 is reset by the next CLK pulse The 40th addition is thus initiated. The ding edge of the $\overline{Q}$ output of the flip-flop 135 sets flip-flop 132 via OR gate 133 to permit the next CLK pulse to: reset the flip flop 132; enter a new e from the ROM; set the JK flip-flop 135 to allow ltiplication to be resumed with the following CLK pulse; and increment the X-register 131 to the dress of the next rate Multiplication then continues before until the decoder 96' stops it after all kilowatt urs have been multiplied by a rate factor, or until the coder/detector 139 stops it momentarily when the h kilowat hours is being multiplied in order to read the next rate together with the number 221 to be d in the decoder/detector 139. When the last rate been read out, the multiplication process continues il the M-register counts down to one. To assure that, egative one is stored with the last rate and read out the decoder/detector which obviously fails to detect egative one as the counter 137 counts up The next CLK pulse initiates the last cycle of adding the last factor in the Q register to the accumulated total in A-register and resets the flip-flop 95'. At the same e, the gate 98' transmits a multiplication complete nal, MCP, to the sequence control section to advance the program counter to T_{39}.

hese embodiments may be modified to accommoe additional factors which make up the monthly bill interjecting additional sequenced operations For mple, if there is to be a minimum of $1.00, the net just computed may be compared at time T_{39}, with minimum, and the larger amount selected as the

amount to be paid That would require only one LFCLK period, and would therefore merely shift all the remaining operations over one timing period of the program counter. Still other operations can be added, such as reading a previous balance from the card and adding it to the current monthly bill. The sum would then be printed as the amount to be paid However, as additional factors are included, the complexity of the system hardware increases It then becomes advantageous to implement as much of the hardware as possible with software That can be done, for example, by including solid-state random access memory (RAM) for storing both instructions and data for a sequence of operations tailored to each customer using standard subroutines stored and called as necessary, such as the billing rate schedule for the customer, minimum billing, previous balance, and so forth. The customer's ID would simply be used to call out the applicable block of instructions and data

Because modifications and variations falling within the spirit of the invention will occur to those skilled in the art, it is not intended that the scope of the invention be determined by the disclosed exemplary embodiments, but rather should be determined by the breadth of the appended claims

What is claimed is:

1. In a portable billing transactor for entering and processing a utility service transaction, and printing a bill on a record medium for immediate delivery to a customer, said service being measured by a meter read by a person for manual entry, said medium having information necessary for computing the bill in predetermined areas, said information including the previous meter reading and a rate code, the combination comprising:

means for accepting said record medium and holding it in a static postion during a billing transaction,

calculating means for performing arithmetic calculations on data coupled thereto under electronic control, said calculating means including first and second arithmetic registers;

means for reading data from different predetermined areas of said record medium at different controlled times;

means for printing data on different predetermined areas of said record medium at different controlled times;

a buffer register for storing said new meter reading,

keyboard means for manually entering said new meter reading into said buffer register for display,

keyboard means for manually producing a print command,

means responsive to said print command for coupling said net meter reading as displayed from said buffer register into said calculating means,

a source of clock pulses,

a ready light and means for displaying said new meter reading entered into said buffer register,

sequence control means including a program counter responsive to said source of clock pulses for automatically controlling said calculating means, reading means and printing means through predetermined coordinated operations once said accepting means has received a record medium in said static position, said coordinated operations comprising

energizing said ready light to call for manual keyboard entry of said new meter reading into said buffer register after said holding means has ac-

cepted said record medium and said record medium is being held in a static position;

energizing said display means to call for a manual keyboard production of said print command to cause said new meter reading to be printed on said record medium and to be coupled into said first one of said arithmetic registers;

reading said previous meter reading from a second predetermined area of said record medium into said second one of said arithmetic registers when printing of said new meter reading has been completed,

computing a difference between said new meter reading and said previous meter reading, and for storing the difference in said first one of said arithmetic registers;

printing said difference in a preselected area of said record medium;

reading said rate code into said calculating means;

computing the amount due from said difference and said rate code;

printing said amount due in a preselected area of said record medium.

2. Apparatus as defined in claim 1 including addressable means in said calculating means for storing a plurality of rate schedules, each rate schedule consisting of a plurality of rate factors accessed in sequence upon addressing said addressable means by a unique code, and wherein said rate code read from said record medium constitutes said unique code, and further including means for multiplying successive predetermined increments of said difference by successive ones of said rate factors in calculating said amount due

3. Apparatus as defined in claim 1 wherein said information prerecorded in predetermined areas includes a customers identification number and said sequence control means includes coordinated control of the operation of reading said customer identification number from a predetermined area, and said apparatus including nonvolatile bulk storage means for recording transaction information including said customer's identification number, previous meter reading new meter reading, difference between said new meter reading and said previous meter reading, and the amount due

4. Apparatus as defined in claim 3 wherein said nonvolatile bulk storage means includes a buffer storage means for temporary storage of said transaction information as it is read from said record medium and as it is computed, and a magnetic tape into which the contents of said buffer storage means is transferred as the last of said coordinated operations under control of said sequence control means

5. Apparatus as defined in claim 3 including addressable means in said calculating means for storing a plurality of rate schedules, each rate schedule consisting of a plurality of rate factors accessed in sequence upon addressing said addressable means by a unique code, and wherein said rate code read from said record medium constitutes said unique code, and further including means for multiplying successive predetermined increments of said difference by successive ones of said rate factors in calculating said amount due

* * * * *

United States Patent [19]

Jones et al.

[11] 3,956,740

[45] May 11, 1976

[54] **PORTABLE DATA ENTRY APPARATUS**

[75] Inventors: Michael Dale Jones; David Alan Johnson; Carl Taylor Wright; William Sherman Bell, Jr., all of Houston, Tex.

[73] Assignee: Telxon Corporation, Houston, Tex.

[22] Filed: Nov. 29, 1974

[21] Appl. No.: 528,441

[52] U.S. Cl. ..... 340/172.5; 360/4; 360/72; 235/61.6 R

[51] Int. Cl.[2] G06F 13/00; G06F 13/04; G11B 5/00; G11B 15/18

[58] Field of Search ..... 340/172.5; 235/152, 235/156, 61.6 R; 360/4, 72

[56] References Cited

UNITED STATES PATENTS

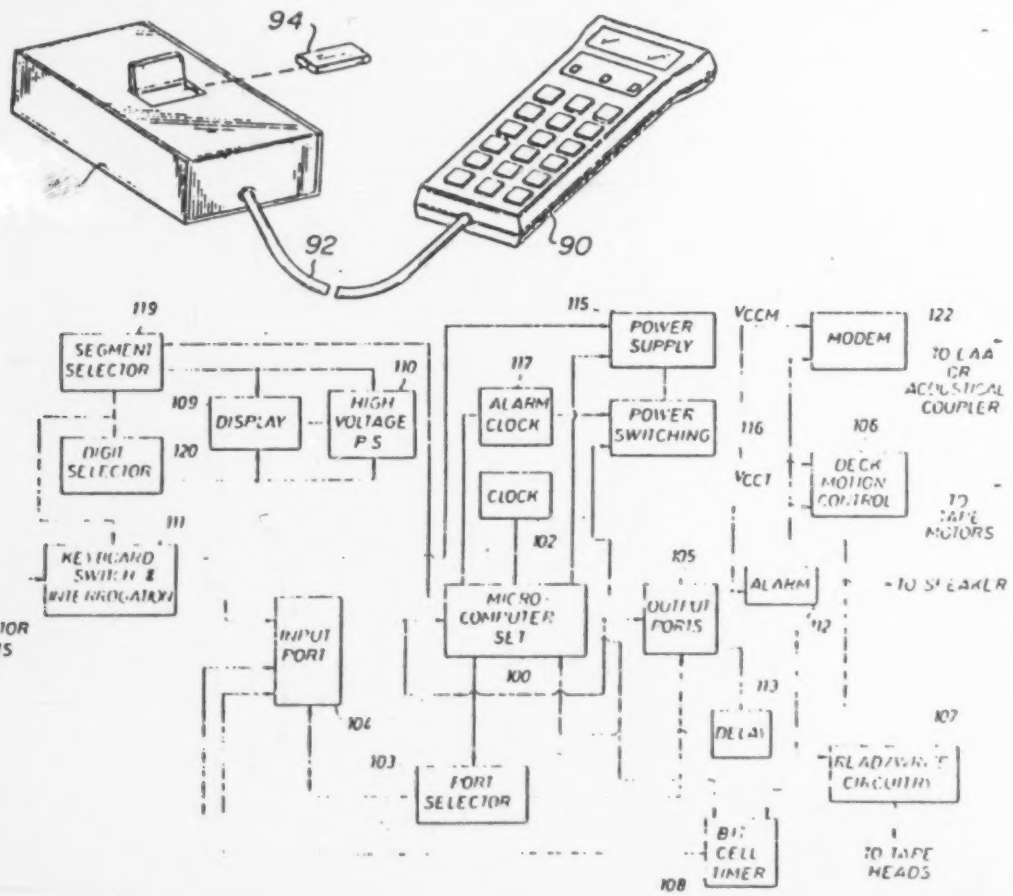
3,594,734	7/1971	Wang	340/172.5
3,748,452	7/1973	Ruben	340/172.5
3,760,171	9/1973	Wang	340/172.5
3,760,375	9/1973	Irwin	340/172.5
3,771,132	11/1973	Biewer	340/172.5
3,819,921	6/1974	Kilby	235/156
3,823,388	7/1974	Chadima	340/172.5

Primary Examiner—Gareth D. Shaw
Assistant Examiner—James D. Thomas
Attorney, Agent, or Firm—Arnold, White & Durkee

[57] ABSTRACT

An improved portable data entry machine is disclosed, wherein data may be keyed, viewed for accuracy, recorded on magnetic tape, recalled from magnetic tape, and telephonically transmitted for data processing. Improvements include a search feature to locate previously recorded data, an automatically controlled power switching unit to prolong the times that batteries may be used prior to recharging, microcomputer controlled circuitry to prevent attempted data entry under low-battery conditions, an electronic shutdown to prevent cell reversal, a voltage reference technique to minimize the power drain from the batteries, a unique mechanism and circuitry to preclude the inadvertent destruction of data, a low cost modem for communicating entered data to a remote location, an automatic interlock for the tape compartment, a highly effective display technique, a novel high voltage power supply, and an out-of-sequence detector.

4 Claims, 26 Drawing Figures



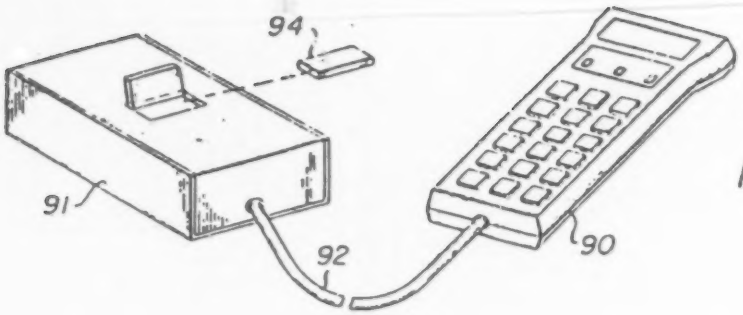
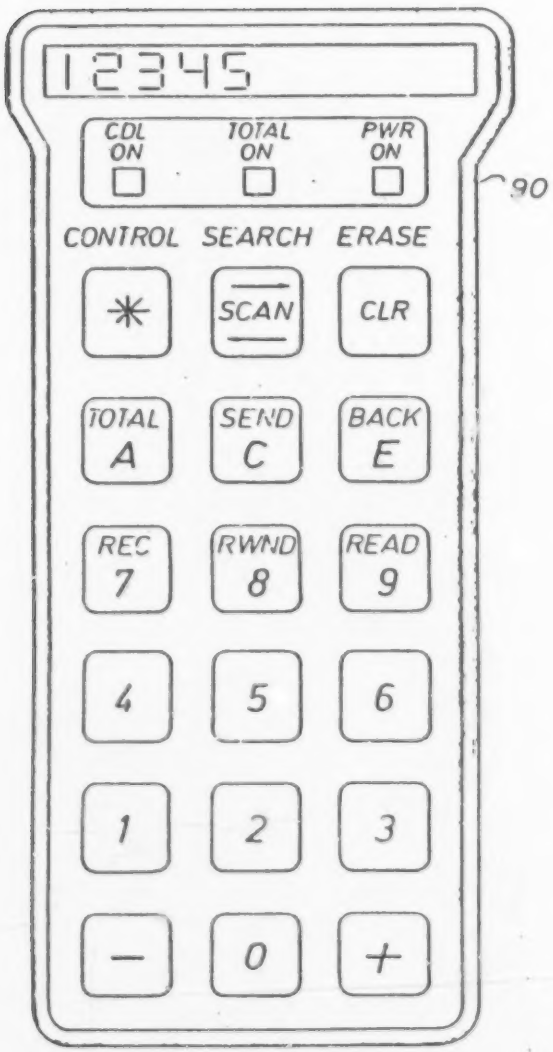

94
91
92
90

FIG. 1

FIG. 1A


12345
CDL ON
TOTAL ON
PWR ON
90
CONTROL
SEARCH
ERASE
✳
SCAN
CLR
TOTAL A
SEND C
BACK E
REC 7
RWND 8
READ 9
4
5
6
1
2
3
−
0
+

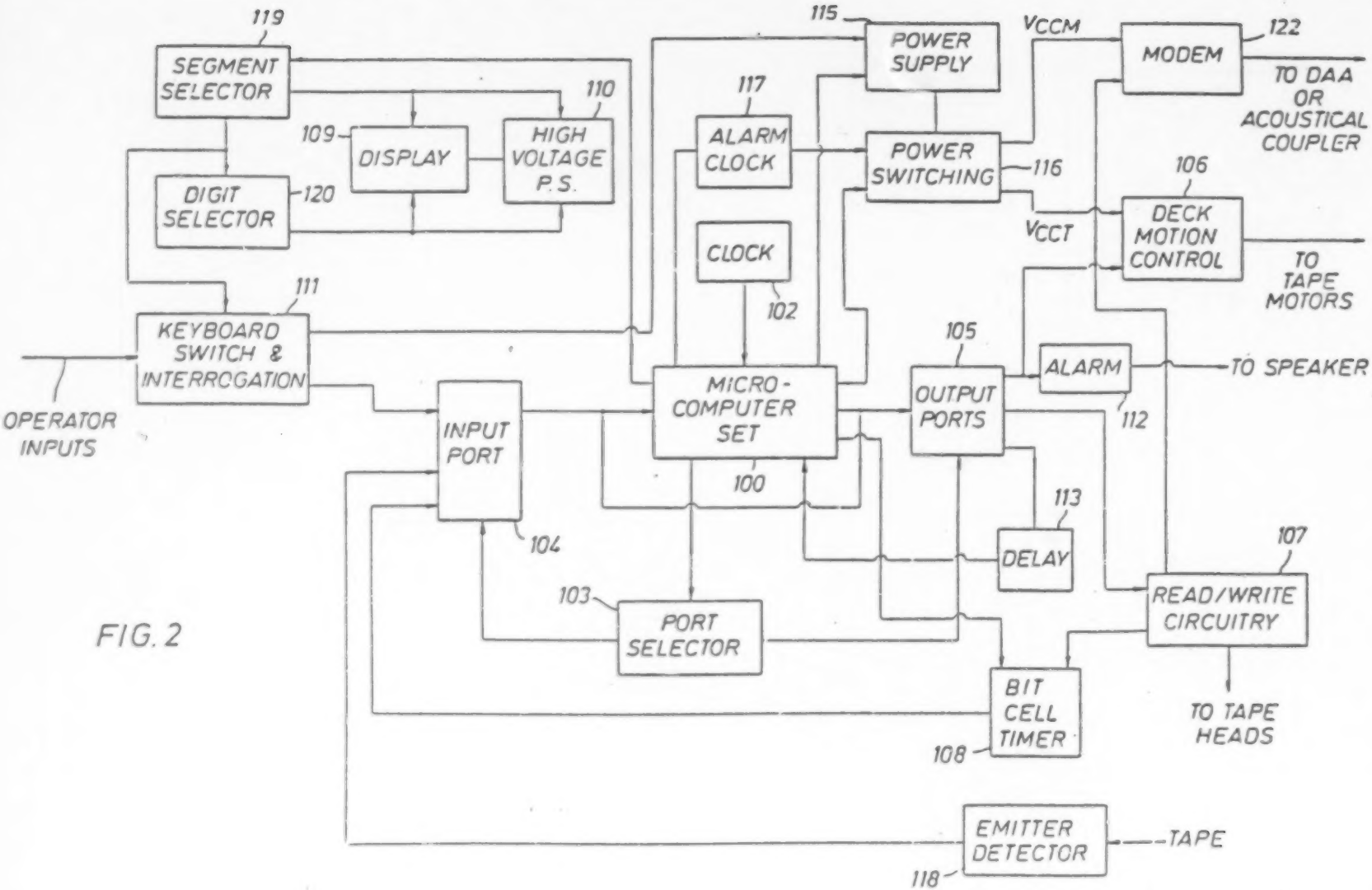

119
SEGMENT SELECTOR
110
109
DISPLAY
HIGH VOLTAGE P.S.
DIGIT SELECTOR
120
111
KEYBOARD SWITCH & INTERROGATION
OPERATOR INPUTS
115
POWER SUPPLY
VCCM
122
MODEM
TO DAA OR ACOUSTICAL COUPLER
117
ALARM CLOCK
POWER SWITCHING
116
106
DECK MOTION CONTROL
VCCT
TO TAPE MOTORS
CLOCK
102
105
ALARM
TO SPEAKER
112
MICRO-COMPUTER SET
OUTPUT PORTS
INPUT PORT
100
113
DELAY
107
104
103
PORT SELECTOR
READ/WRITE CIRCUITRY
BIT CELL TIMER
TO TAPE HEADS
108
EMITTER DETECTOR
TAPE
118

FIG. 2

FIG. 3

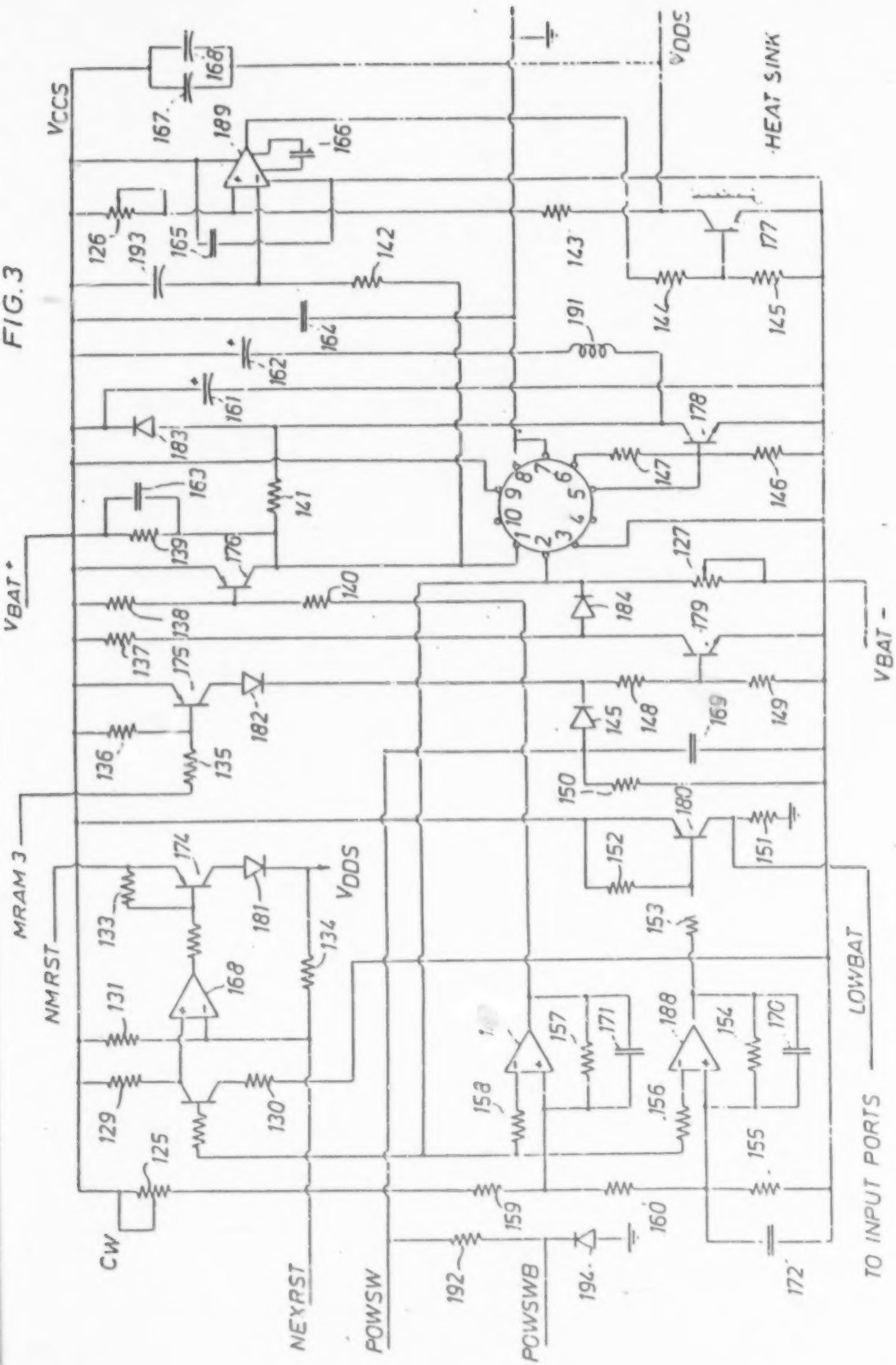
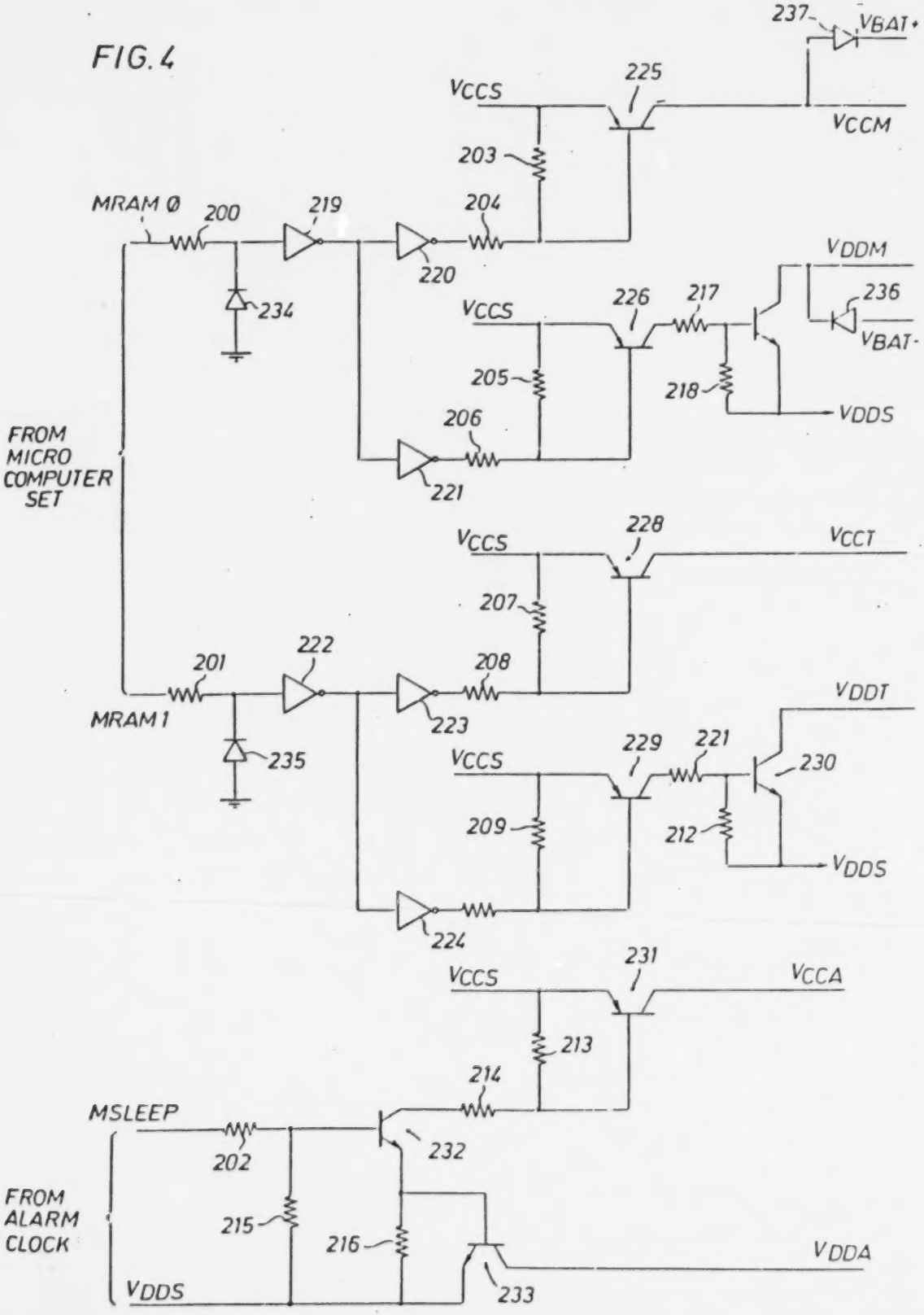

VCCS
VDDS
HEAT SINK
VBAT +
VBAT -
MRAM 3
NMRST
CW
NEXRST
POWSW
POWSWB
LOWBAT
TO INPUT PORTS

FIG. 4


237
VBAT+
225
VCCS
VCCM
203
MRAM 0
200
219
204
220
VDDM
234
226
217
236
VCCS
VBAT-
205
218
VDDS
206
FROM MICRO COMPUTER SET
221
228
VCCS
VCCT
207
222
201
208
MRAM 1
223
VDDT
235
229
221
VCCS
230
209
212
VDDS
224
231
VCCS
VCCA
213
214
MSLEEP
232
202
FROM ALARM CLOCK
215
216
VDDA
VDDS
233

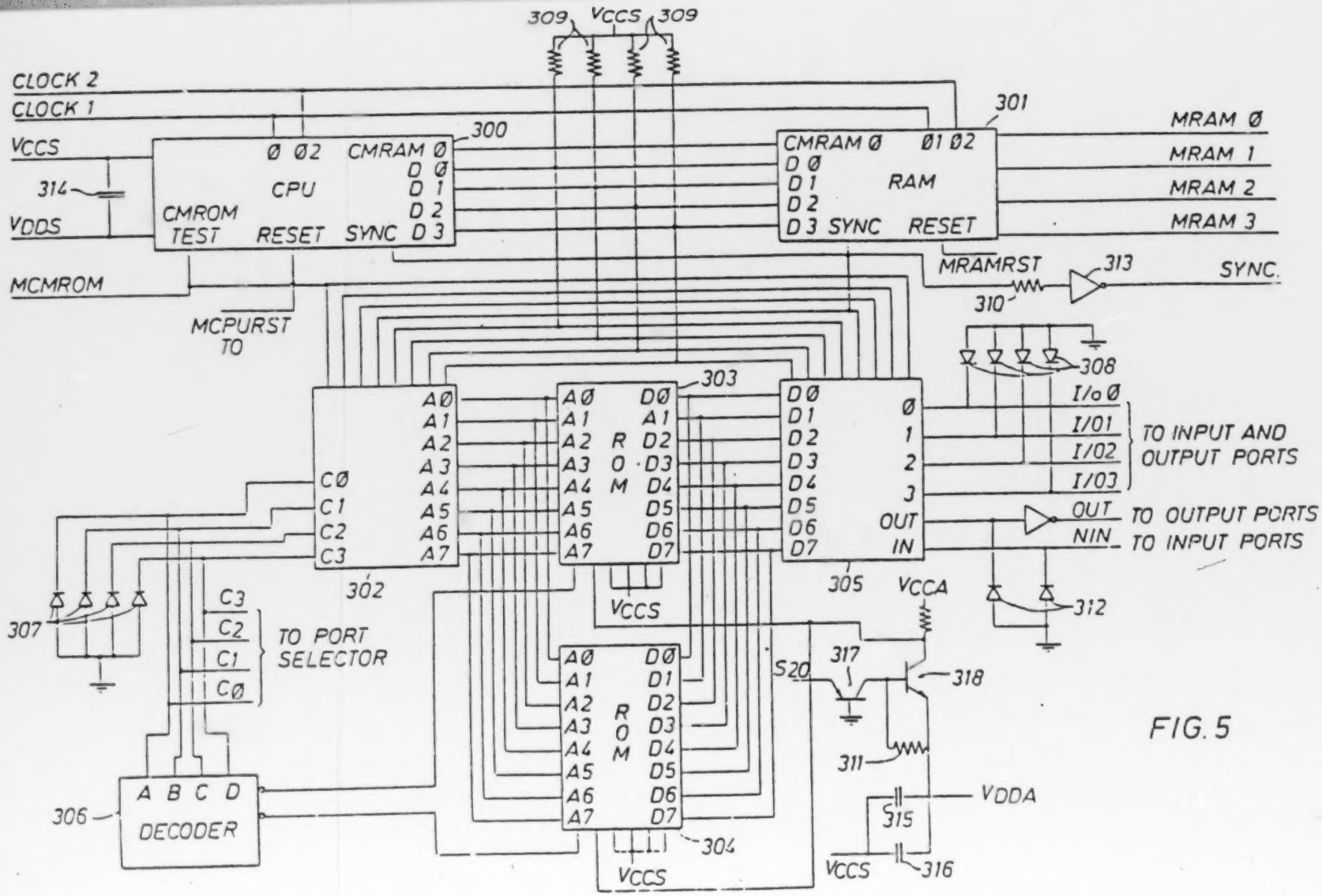

309
VCCS
309
CLOCK 2
CLOCK 1
VCCS
314
VDDS
300
Ø Ø2
CPU
CMRAM Ø
D Ø
D 1
D 2
D 3
CMROM TEST
RESET
SYNC
301
CMRAM Ø
Ø1 Ø2
D Ø
D 1
D 2
D 3 SYNC
RAM
RESET
MRAM Ø
MRAM 1
MRAM 2
MRAM 3
MRAMRST
313
SYNC.
310
MCMROM
MCPURST TO
308
I/o Ø
I/01
I/02
I/03
TO INPUT AND OUTPUT PORTS
OUT
NIN
TO OUTPUT PORTS
TO INPUT PORTS
303
A Ø
A 1
A 2
A 3
A 4
A 5
A 6
A 7
R O M
D Ø
D 1
D 2
D 3
D 4
D 5
D 6
D 7
C Ø
C 1
C 2
C 3
302
305
VCCA
312
307
C3
C2
C1
C Ø
TO PORT SELECTOR
VCCS
317
318
S20
311
A B C D
DECODER
306
304
VDDA
315
VCCS
316

FIG. 5

200

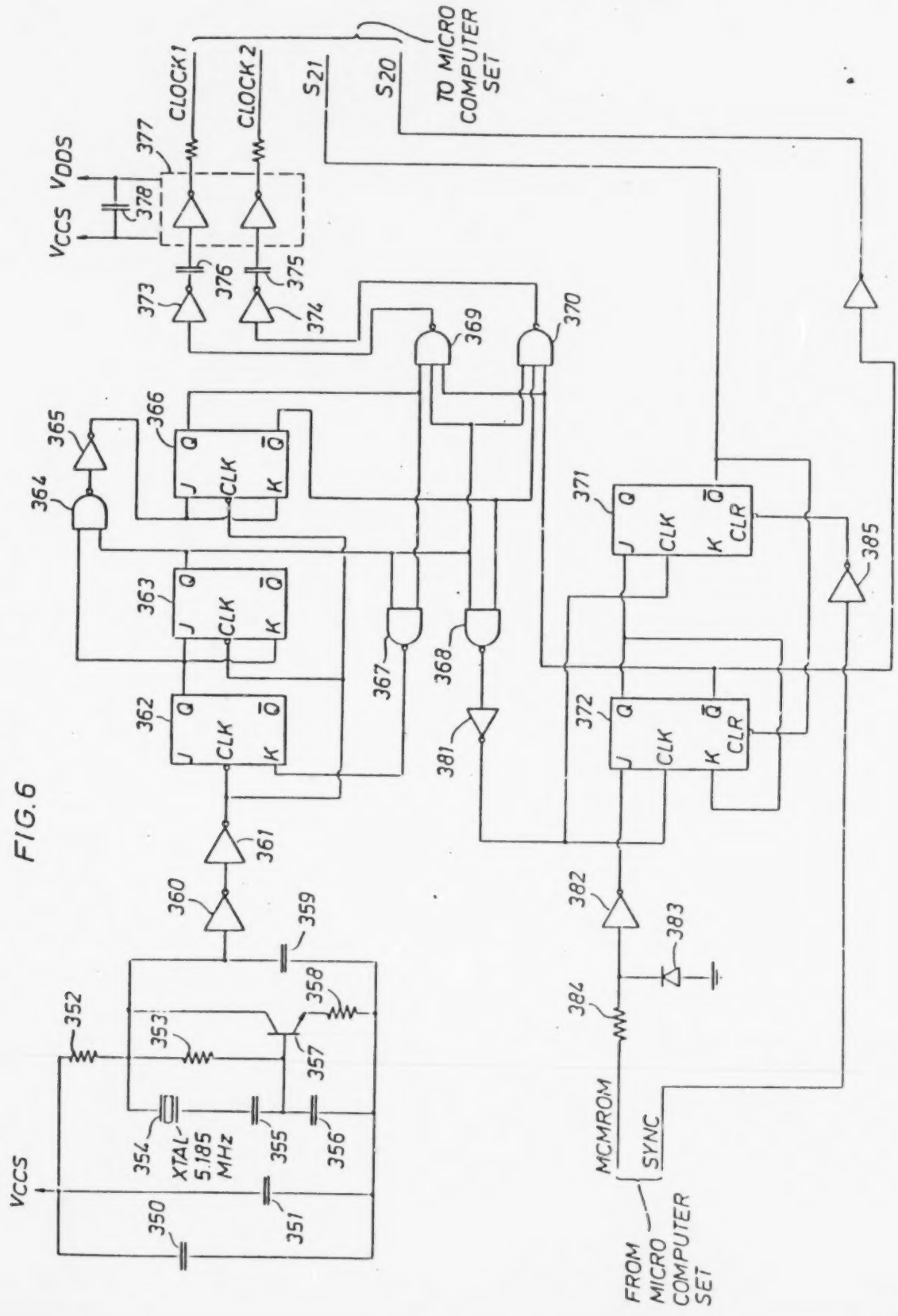

TO MICRO COMPUTER SET
S20
S21
CLOCK1
CLOCK2
377
378
VCCS VDDS
373
374
375
376
369
370
365
366
364
363
362
367
368
371
372
385
381
361
360
359
358
352
353
357
354
355
356
350
351
XTAL 5.185 MHz
VCCS
382
383
384
MCMROM
SYNC
FROM MICRO COMPUTER SET

FIG.6

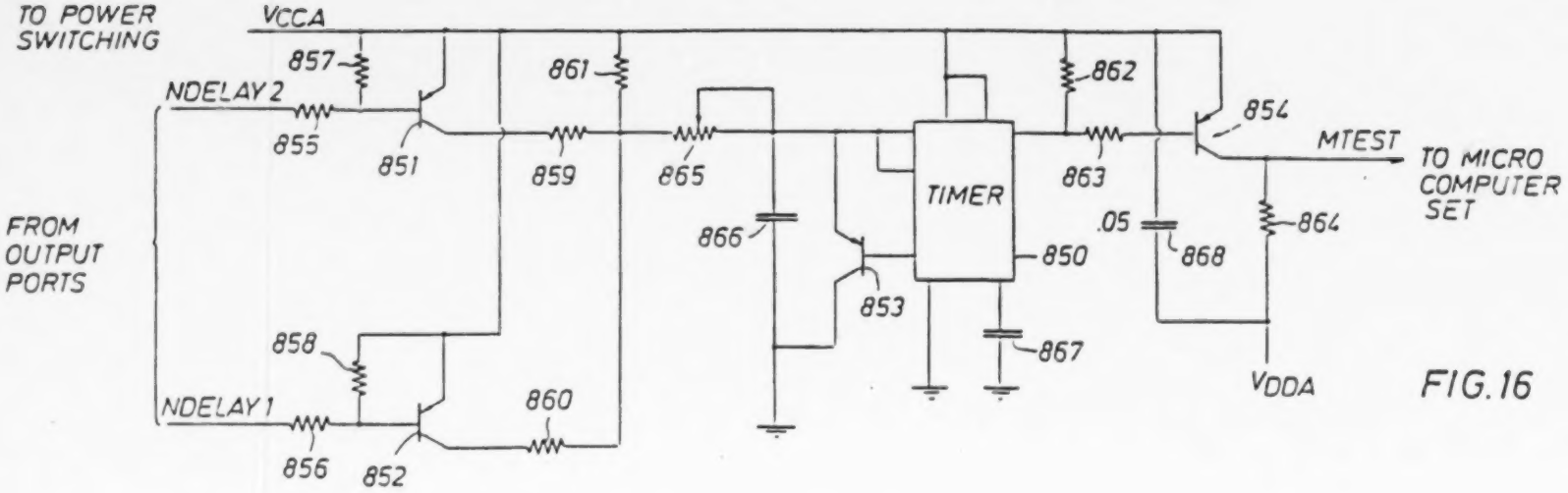


FIG. 16

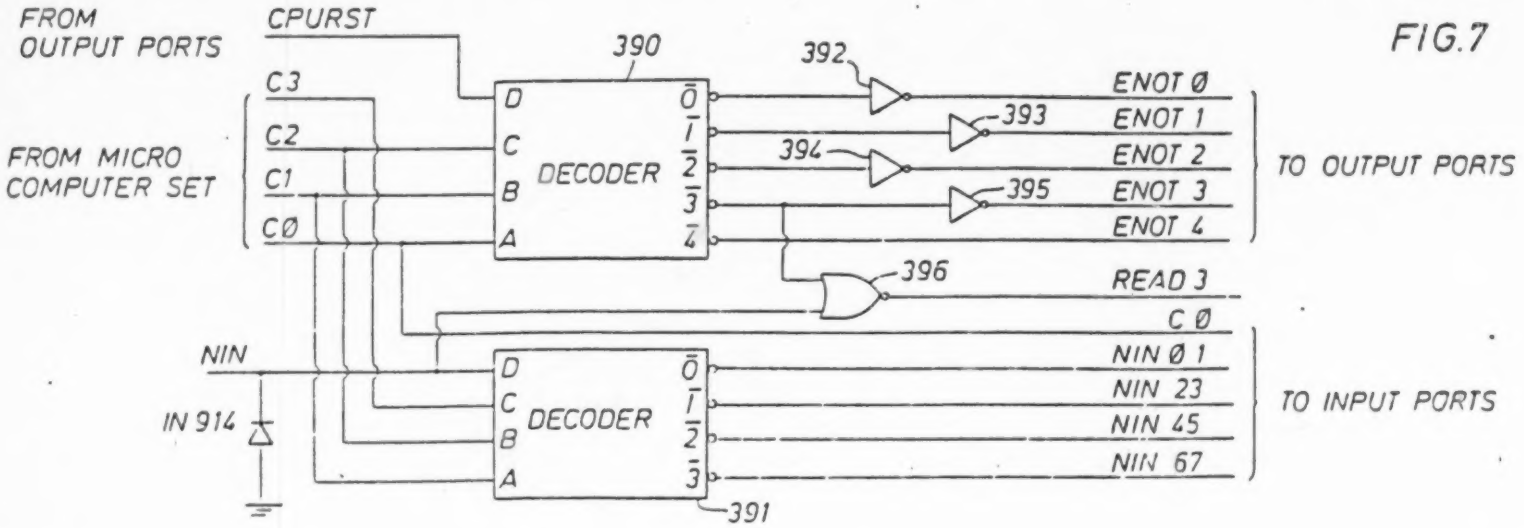
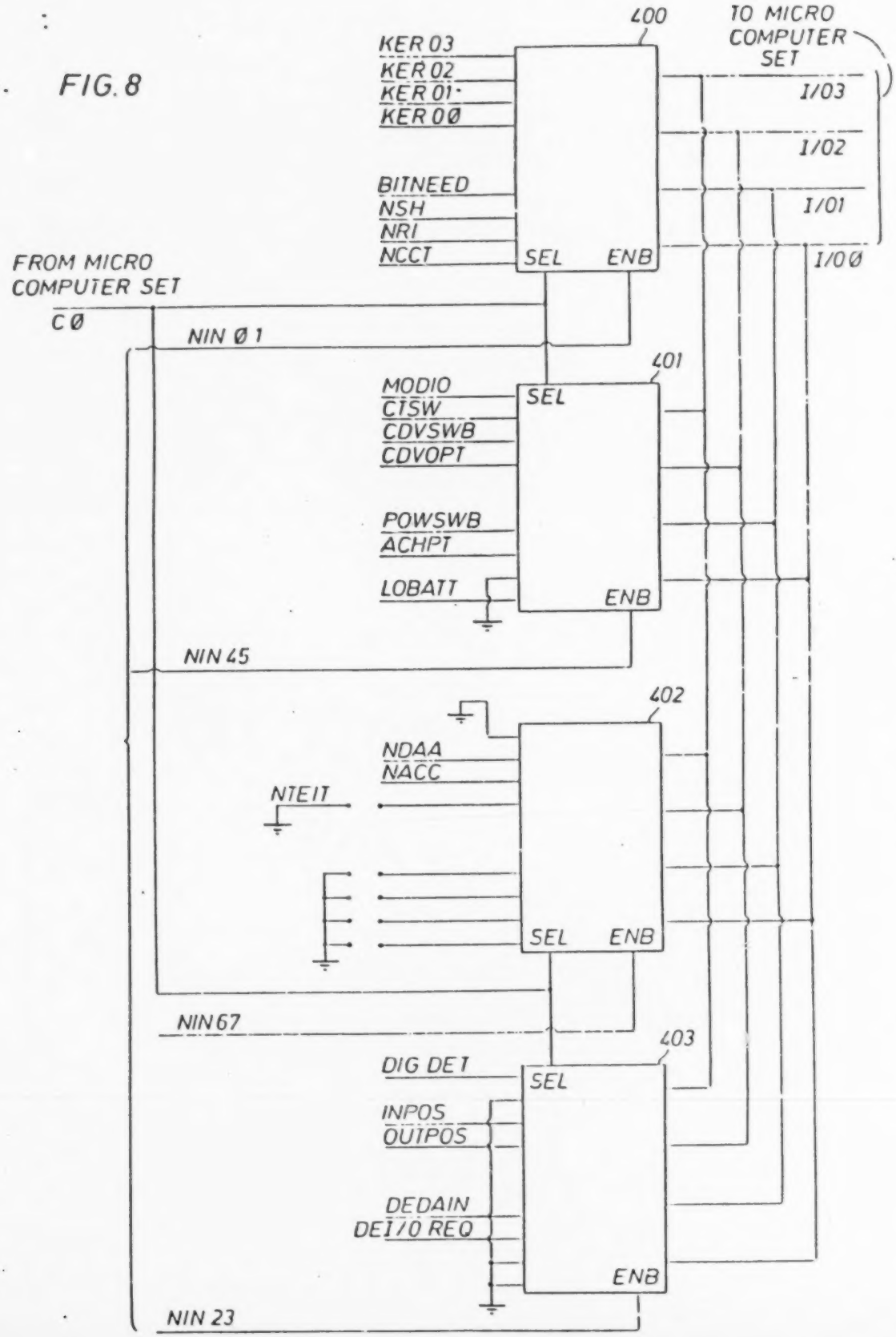


FIG. 7

004

FIG. 8


400
TO MICRO COMPUTER SET
KER 03
KER 02
KER 01
KER 00
BITNEED
NSH
NRI
NCCT
SEL
ENB
I/03
I/02
I/01
I/00
FROM MICRO COMPUTER SET
C0
NIN 01
401
MODIO
CTSW
CDVSWB
CDVOPT
POWSWB
ACHPT
LOBATT
SEL
ENB
NIN 45
402
NDAA
NACC
NTEIT
SEL
ENB
NIN 67
403
DIG DET
INPOS
OUTPOS
DEDAIN
DET/O REQ
SEL
ENB
NIN 23

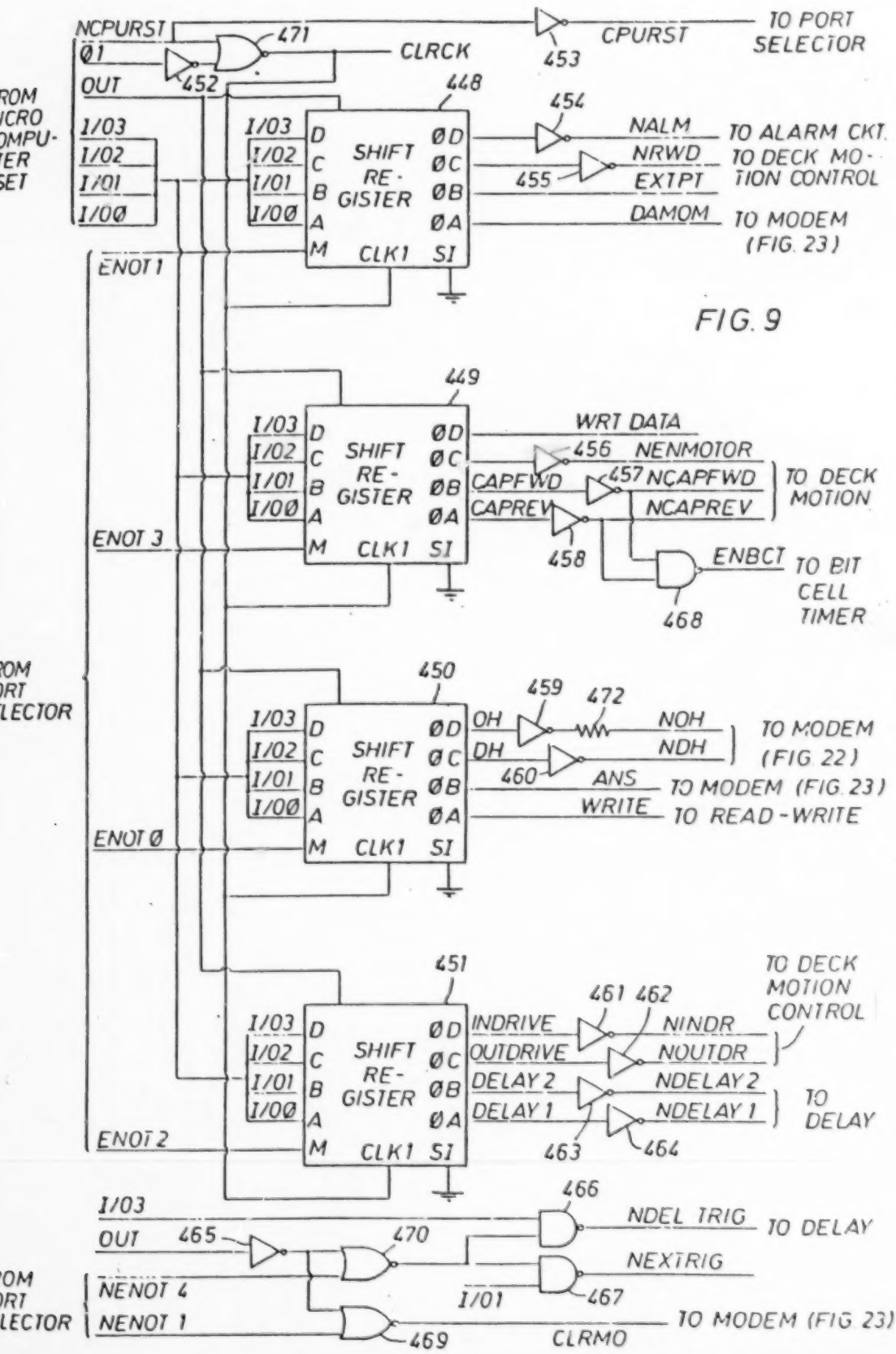
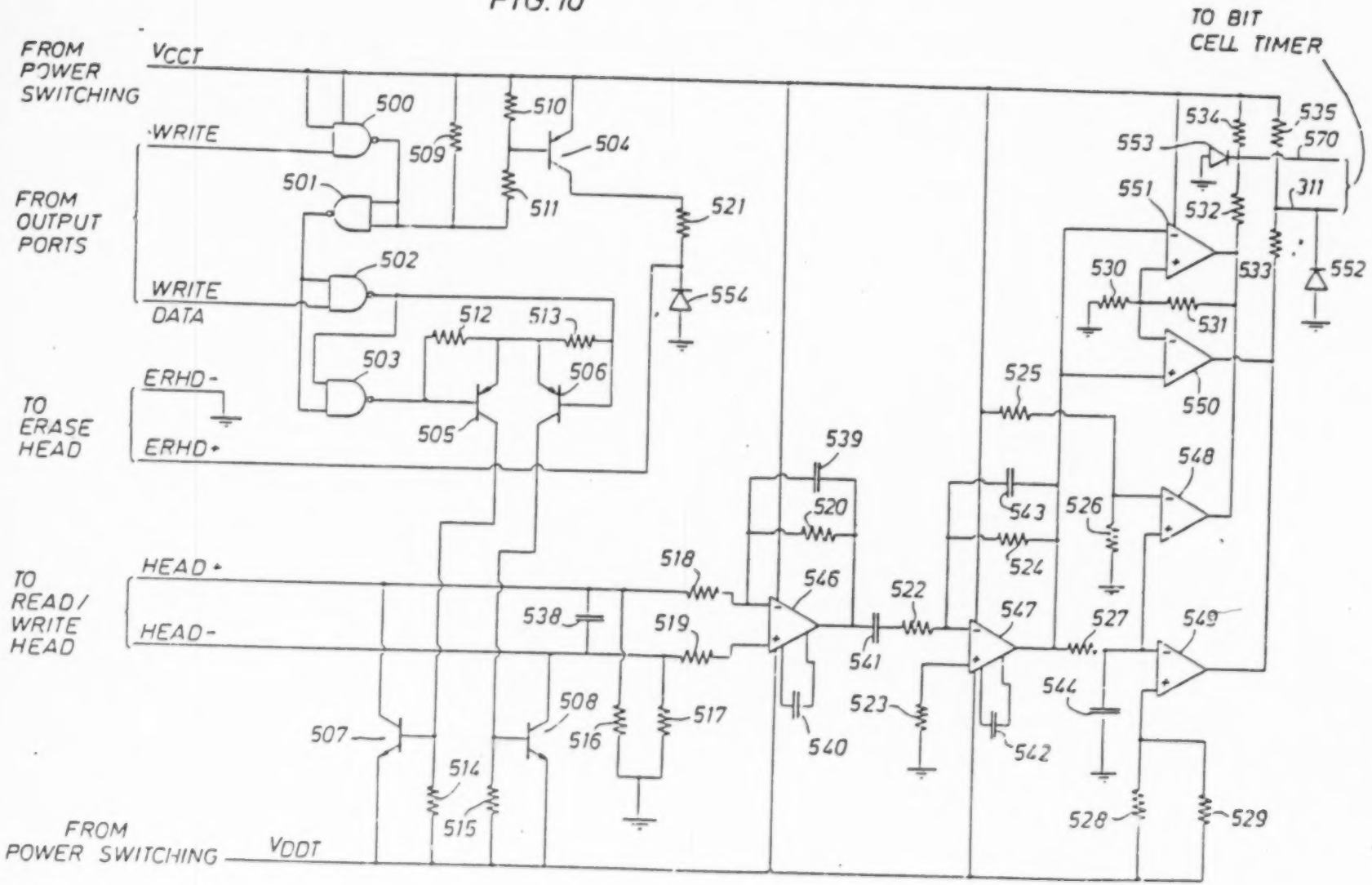

NCPURST
Ø1
OUT
471
452
CLRCK
453
CPURST
TO PORT SELECTOR
448
454
NALM
TO ALARM CKT.
NRWD
TO DECK MOTION CONTROL
455
EXTPT
DAMOM
TO MODEM (FIG. 23)
I/03
I/02
I/01
I/00
D
C
B
A
M
SHIFT RE-GISTER
ØD
ØC
ØB
ØA
CLK1
SI
ENOT 1
449
WRT DATA
456 NENMOTOR
CAPFWD
457 NCAPFWD
CAPREV
NCAPREV
458
ENBCT
468
TO BIT CELL TIMER
ENOT 3
450
459
472
OH
NOH
DH
NDH
TO MODEM (FIG. 22)
460
ANS
TO MODEM (FIG. 23)
WRITE
TO READ-WRITE
ENOT Ø
451
TO DECK MOTION CONTROL
461 462
INDRIVE
NINDR
OUTDRIVE
NOUTDR
DELAY 2
NDELAY 2
DELAY 1
NDELAY 1
TO DELAY
463
464
ENOT 2
466
NDEL TRIG
TO DELAY
465
470
NEXTRIG
NENOT 4
NENOT 1
I/01
467
469
CLRMO
TO MODEM (FIG 23)

FIG. 9

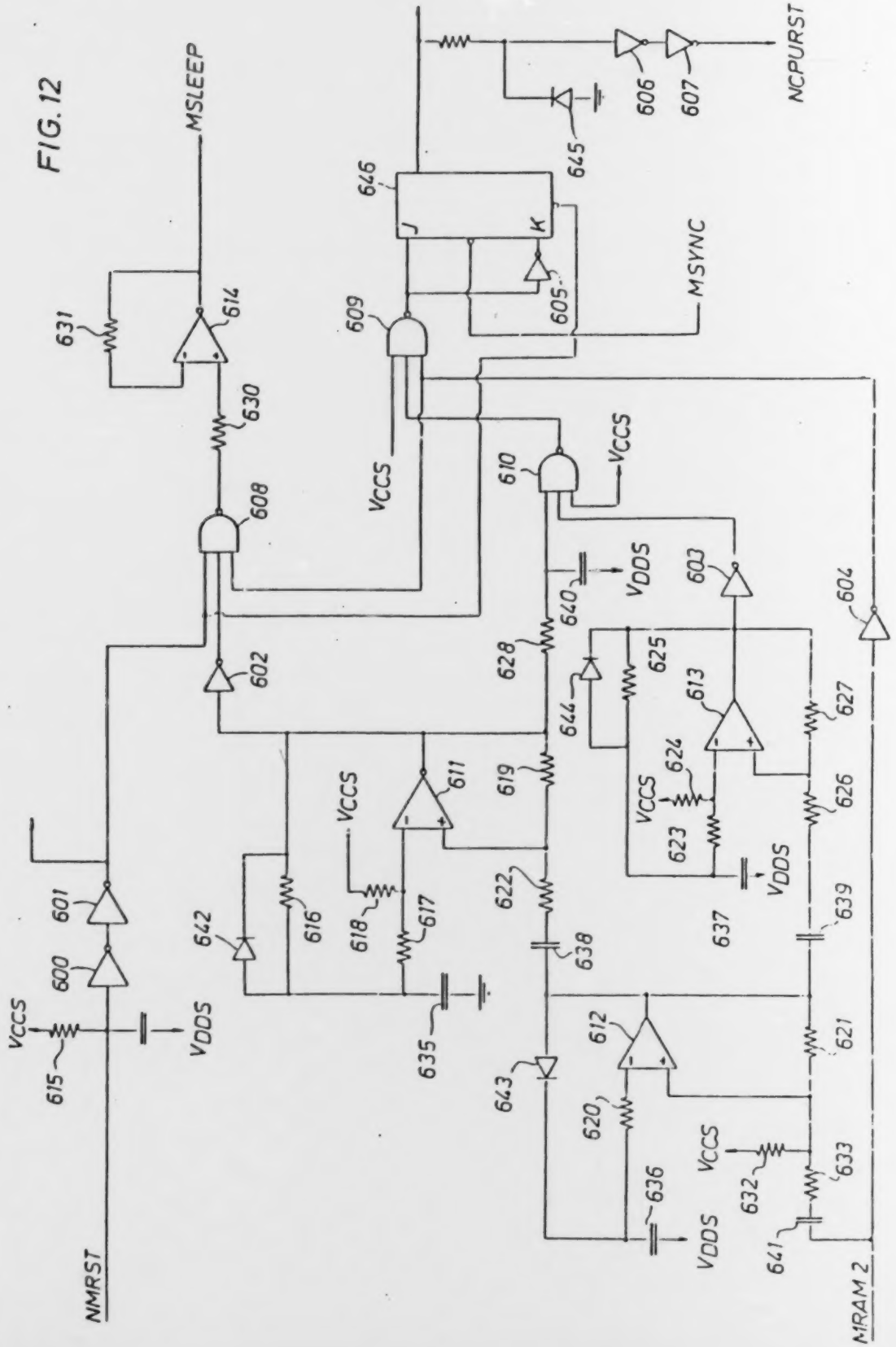
FIG. 10


FROM POWER SWITCHING
VCCT
TO BIT CELL TIMER
WRITE
FROM OUTPUT PORTS
WRITE DATA
ERHD-
TO ERASE HEAD
ERHD+
HEAD+
TO READ/ WRITE HEAD
HEAD-
FROM POWER SWITCHING
VDDT
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
538
539
540
541
542
543
544
546
547
548
549
550
551
552
553
554
570
311

1163
1118
1162
1117
1161
1160
1116
1159
1113
1154
1180
1153
1111
1155
1152
1172
1125
1171
1112
1149
1108
1178
1176
1150
1151
1110
1145
1179
1148
1107
1147
1170
1109
1145
1106
1176
1143
1105
1144
1141
1133
1142
1131
1130
1177
1134
1140
1103
1104
1132
1139
1135
1101
1102
1100
1138
1136
1137
1166
1120
1165
1164
1119
1168
1167
1115
1157
1158
1175
1174
1126
1114
1173

FIG. 11

FIG. 12


MSLEEP
NCPURST
MSYNC
NMRST
MIRAM 2
VCCS
VDDS
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
630
631
632
633
635
636
637
638
639
640
641
642
643
644
645
646
J
K

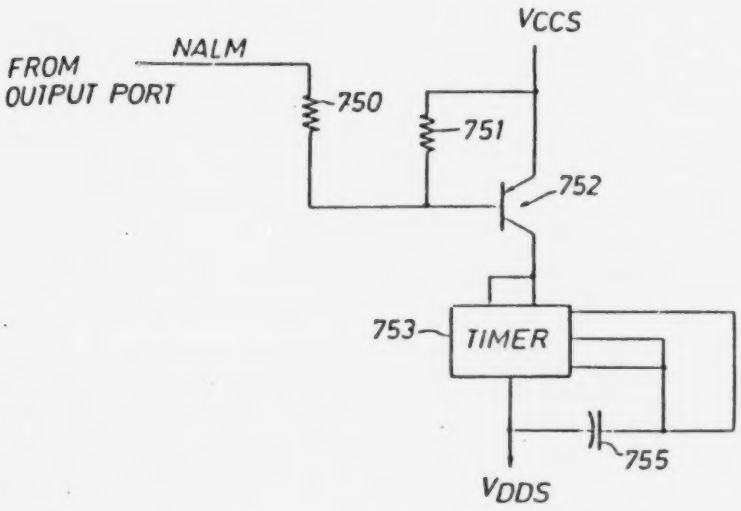

VCCS
NALM
FROM
OUTPUT PORT
750
751
752
753
TIMER
755
VDDS

FIG. 13

FIG. 15

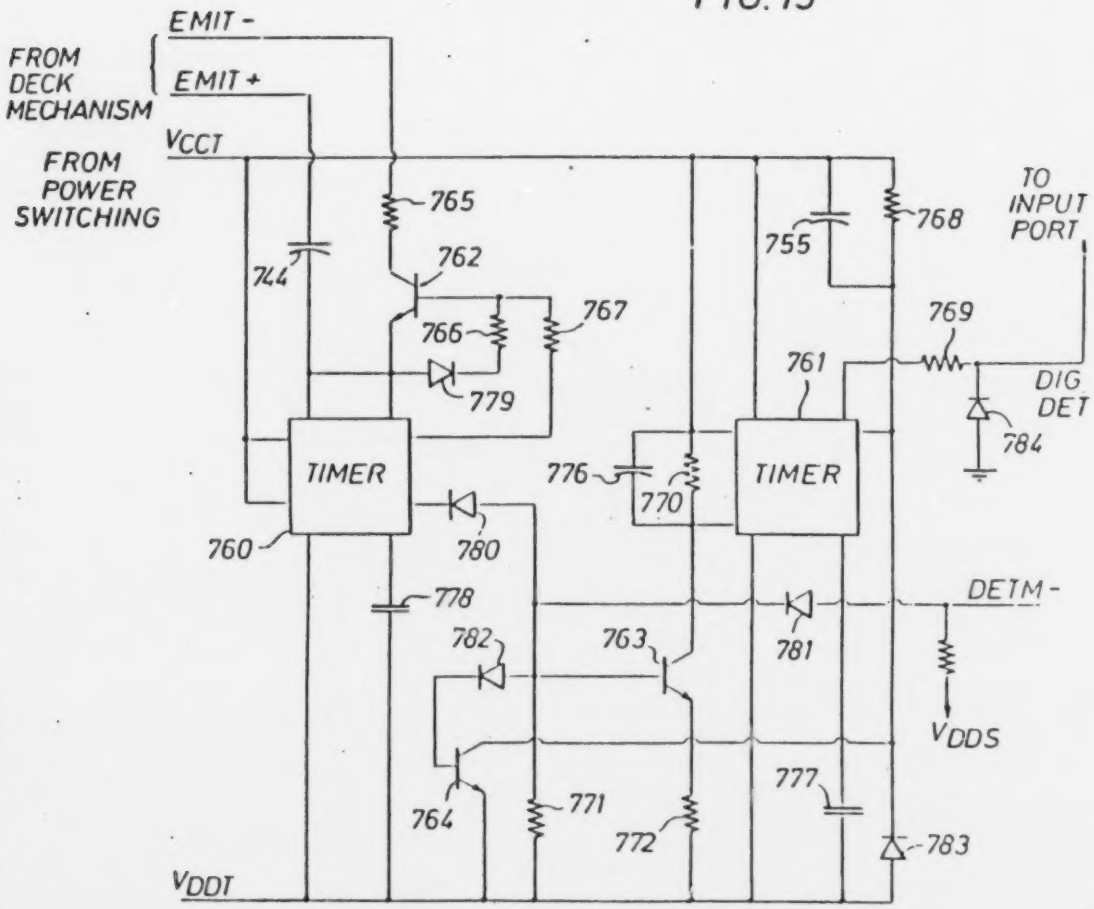
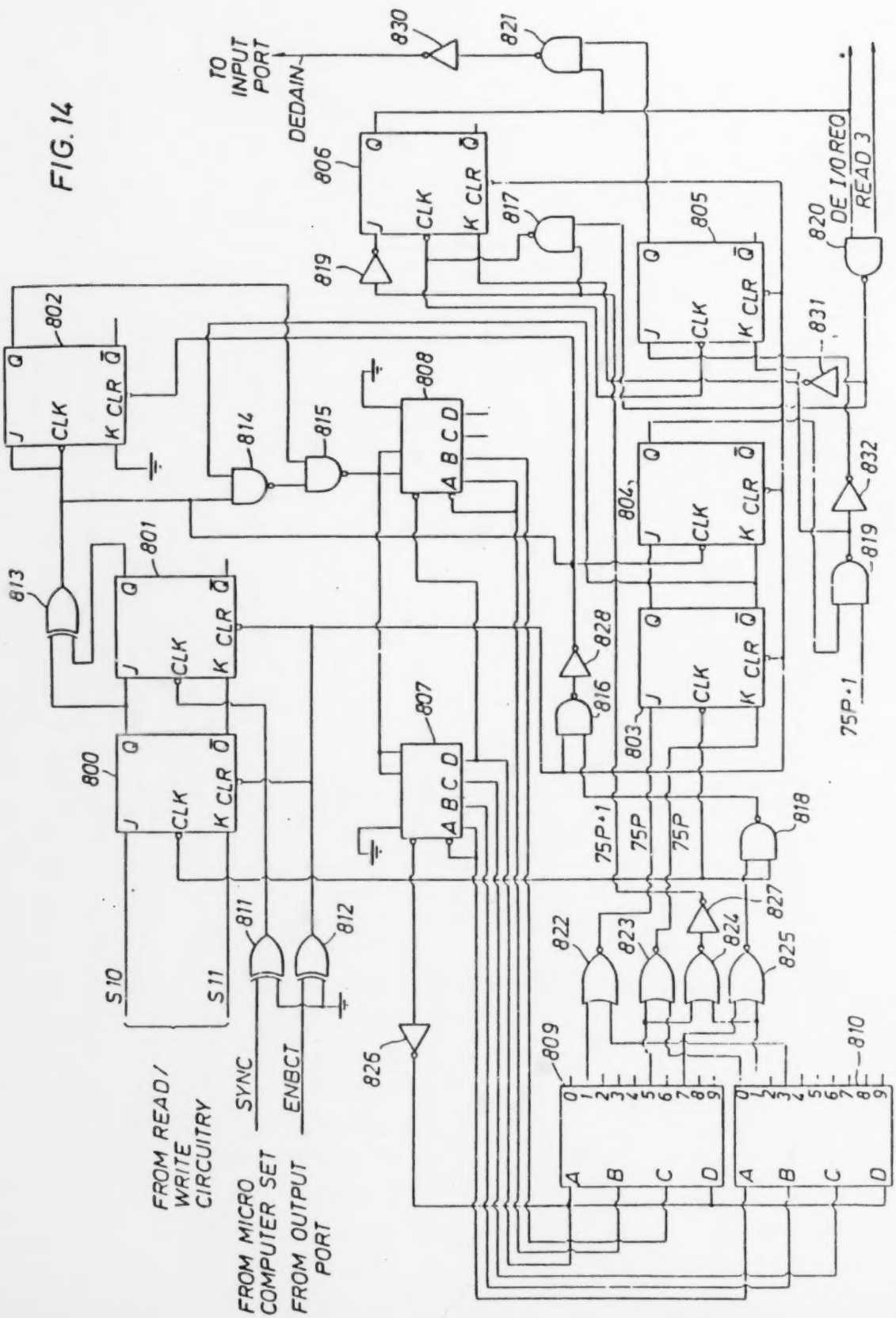

EMIT -
FROM
DECK
MECHANISM
EMIT +
VCCT
FROM
POWER
SWITCHING
765
762
744
766
767
779
TIMER
760
780
778
782
763
764
771
772
TIMER
776
770
755
768
TO
INPUT
PORT
769
761
DIG
DET
784
DETM -
781
VDDS
777
783
VDDT

FIG. 14


TO INPUT PORT
DEDAIN
DE I/O REQ
READ 3
FROM READ/ WRITE CIRCUITRY
FROM MICRO COMPUTER SET
FROM OUTPUT PORT
SYNC
ENBCT
S10
S11
75P·1
75P
CLK
K CLR

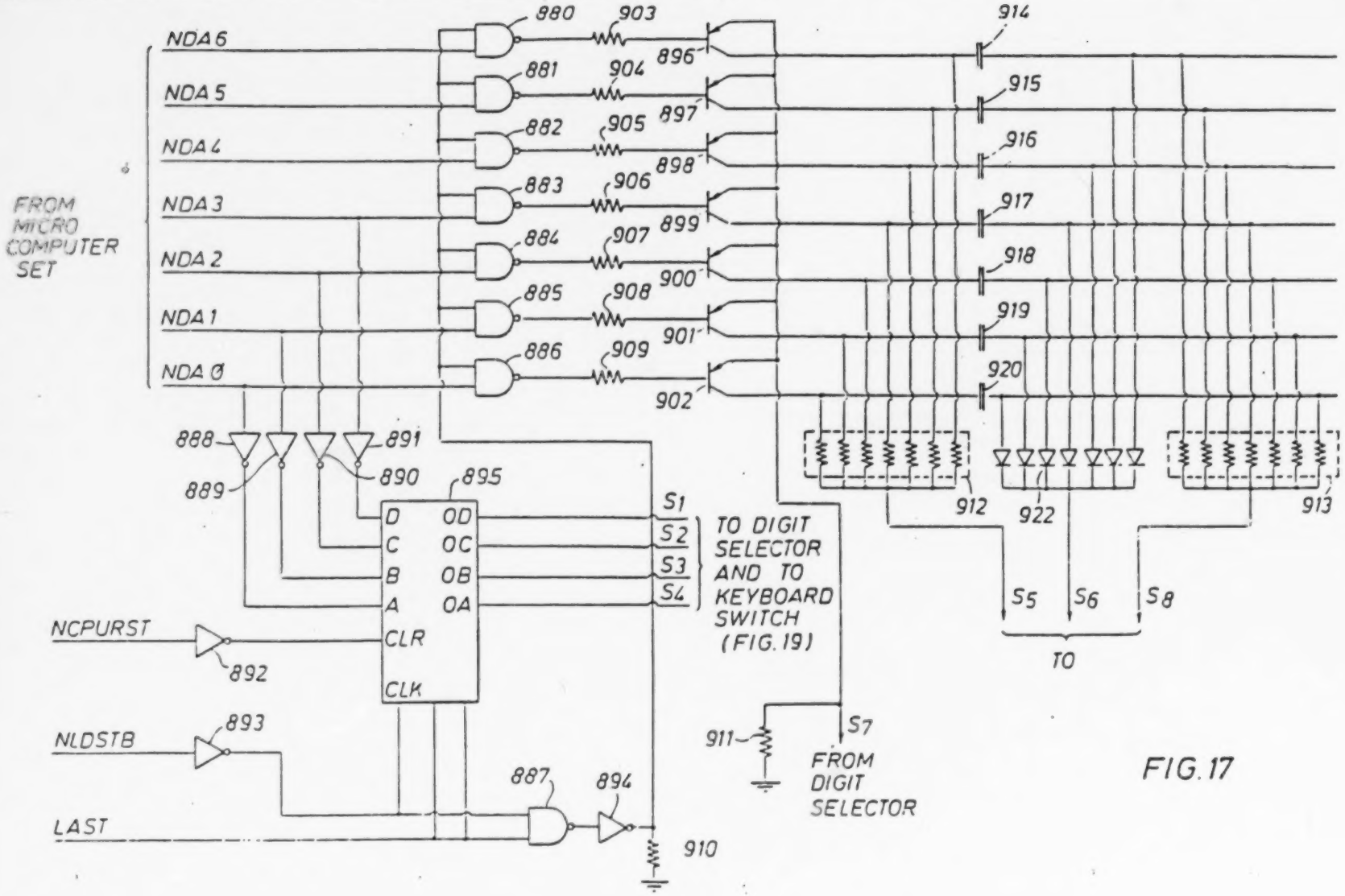

NDA 6
NDA 5
NDA 4
NDA 3
NDA 2
NDA 1
NDA 0
FROM MICRO COMPUTER SET
880
881
882
883
884
885
886
903
904
905
906
907
908
909
896
897
898
899
900
901
902
914
915
916
917
918
919
920
888
889
890
891
895
D
C
B
A
CLR
CLK
OD
OC
OB
OA
S1
S2
S3
S4
TO DIGIT SELECTOR AND TO KEYBOARD SWITCH (FIG. 19)
NCPURST
892
NLDSTB
893
LAST
887
894
910
911
S7
FROM DIGIT SELECTOR
912
922
913
S5
S6
S8
TO

FIG. 17

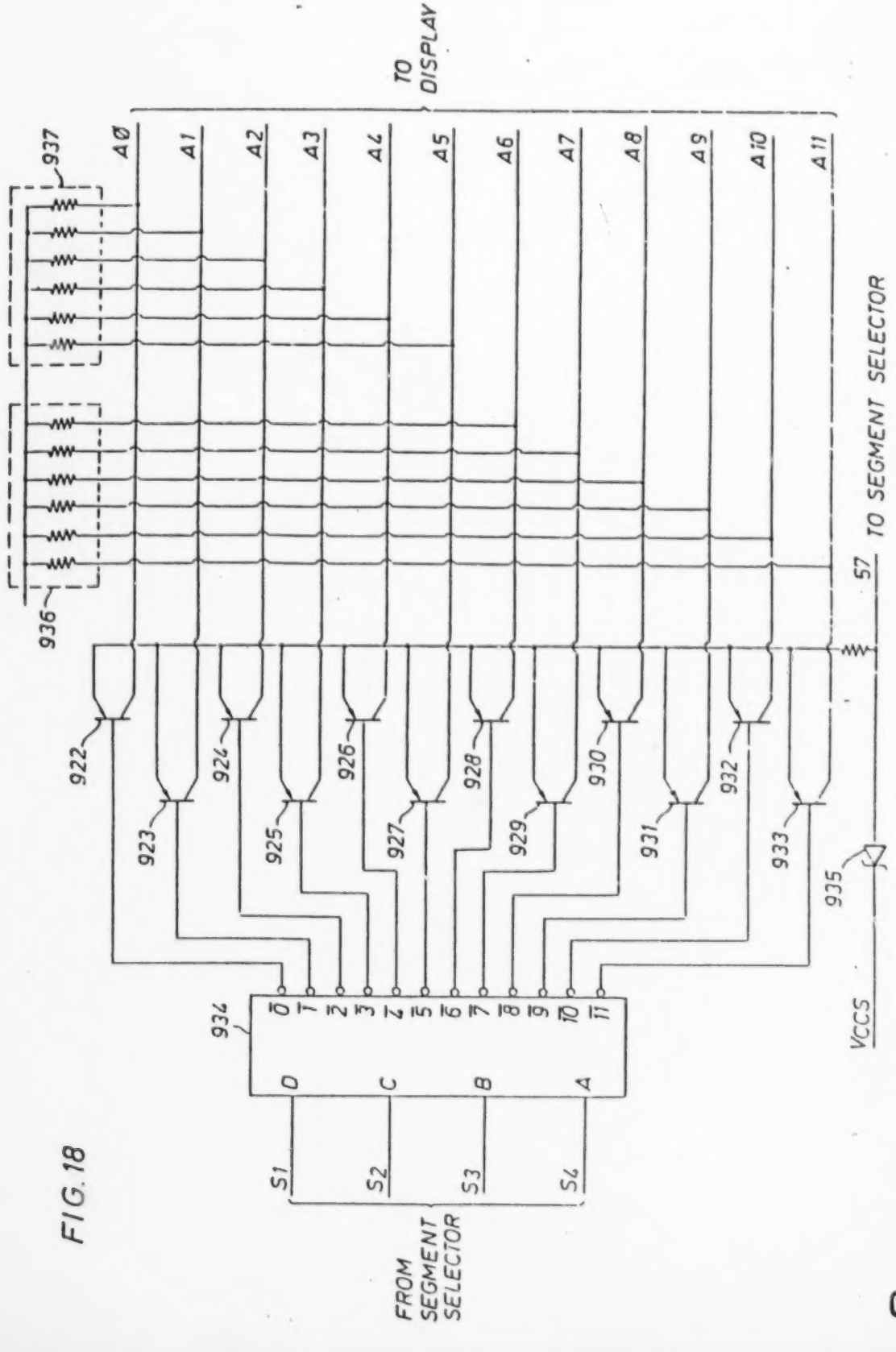

TO DISPLAY
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
937
936
922
923
924
925
926
927
928
929
930
931
932
933
935
57
TO SEGMENT SELECTOR
VCCS
934
0
1
2
3
4
5
6
7
8
9
10
11
D
C
B
A
S1
S2
S3
S4
FROM SEGMENT SELECTOR

FIG. 18

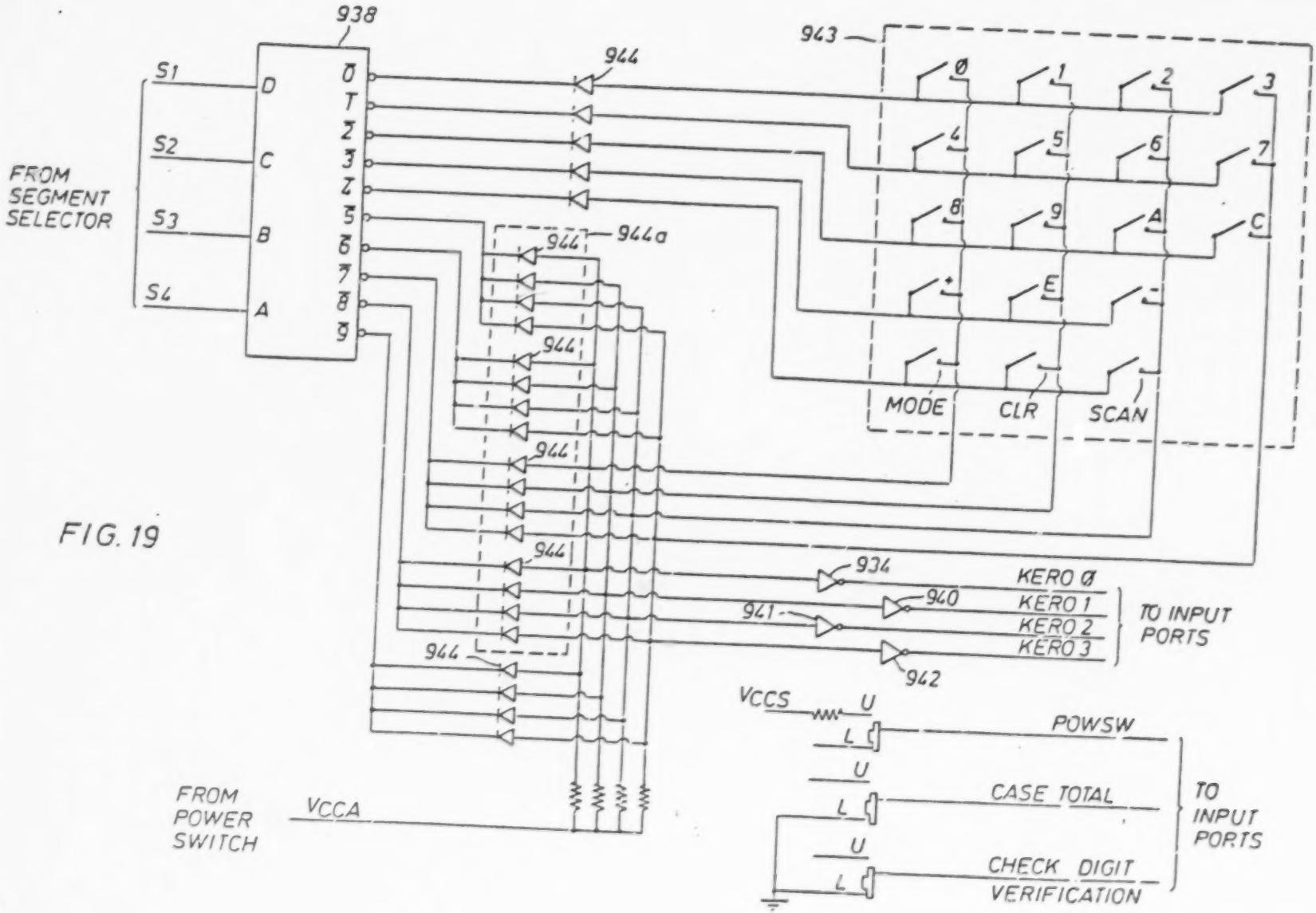

938
943
944
944a
FROM SEGMENT SELECTOR
S1
S2
S3
S4
D
C
B
A
0
1
2
3
4
5
6
7
8
9
MODE
CLR
SCAN
934
940
941
942
KERO 0
KERO 1
KERO 2
KERO 3
TO INPUT PORTS
VCCS
U
L
POWSW
CASE TOTAL
CHECK DIGIT VERIFICATION
FROM POWER SWITCH
VCCA

FIG. 19

FIG. 20

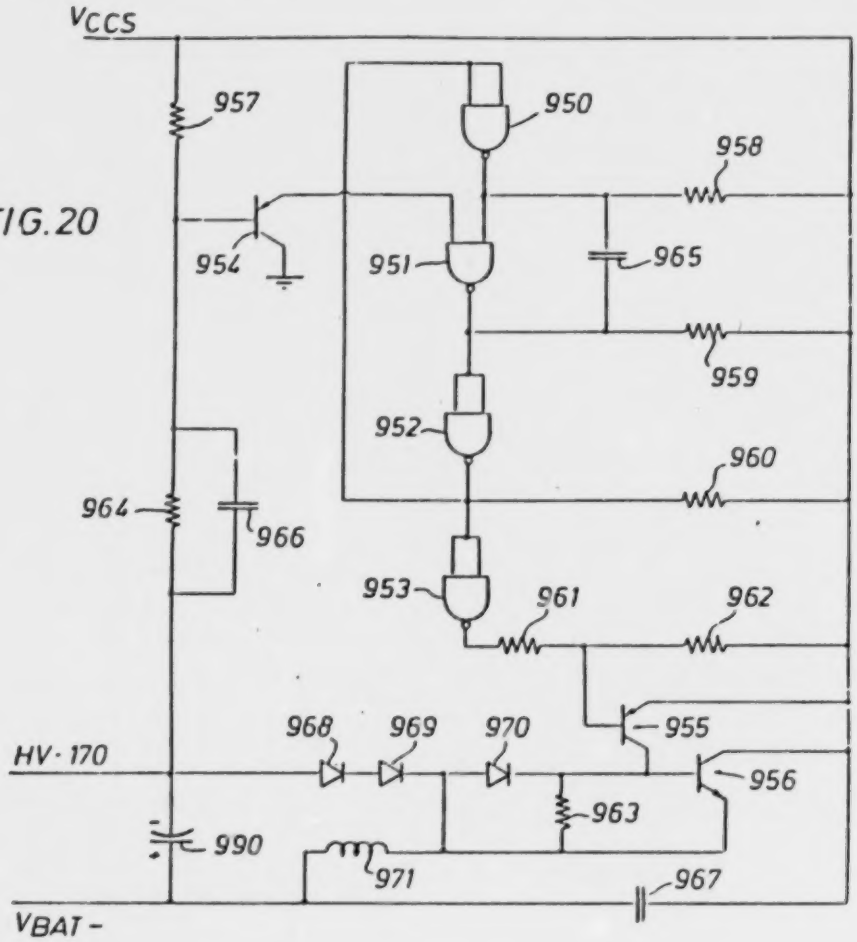


FIG. 20A

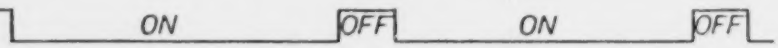
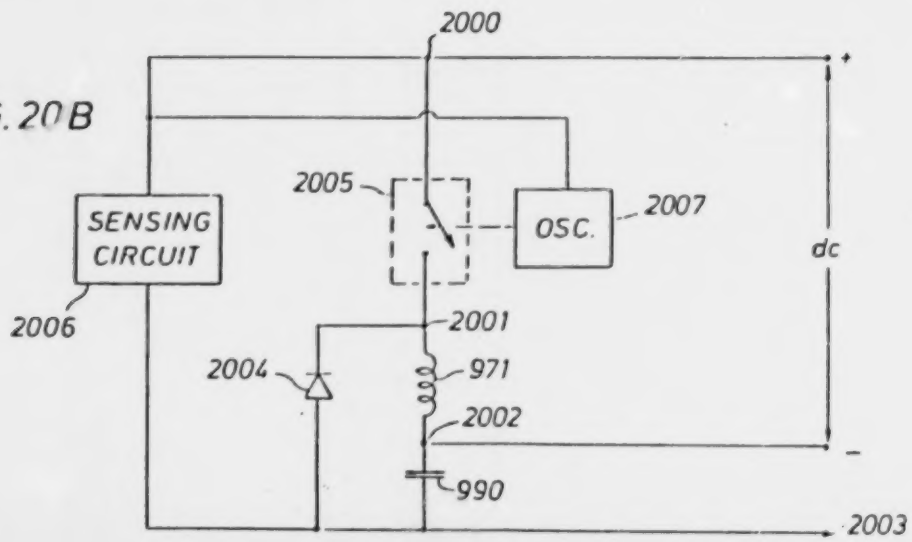


FIG. 20B



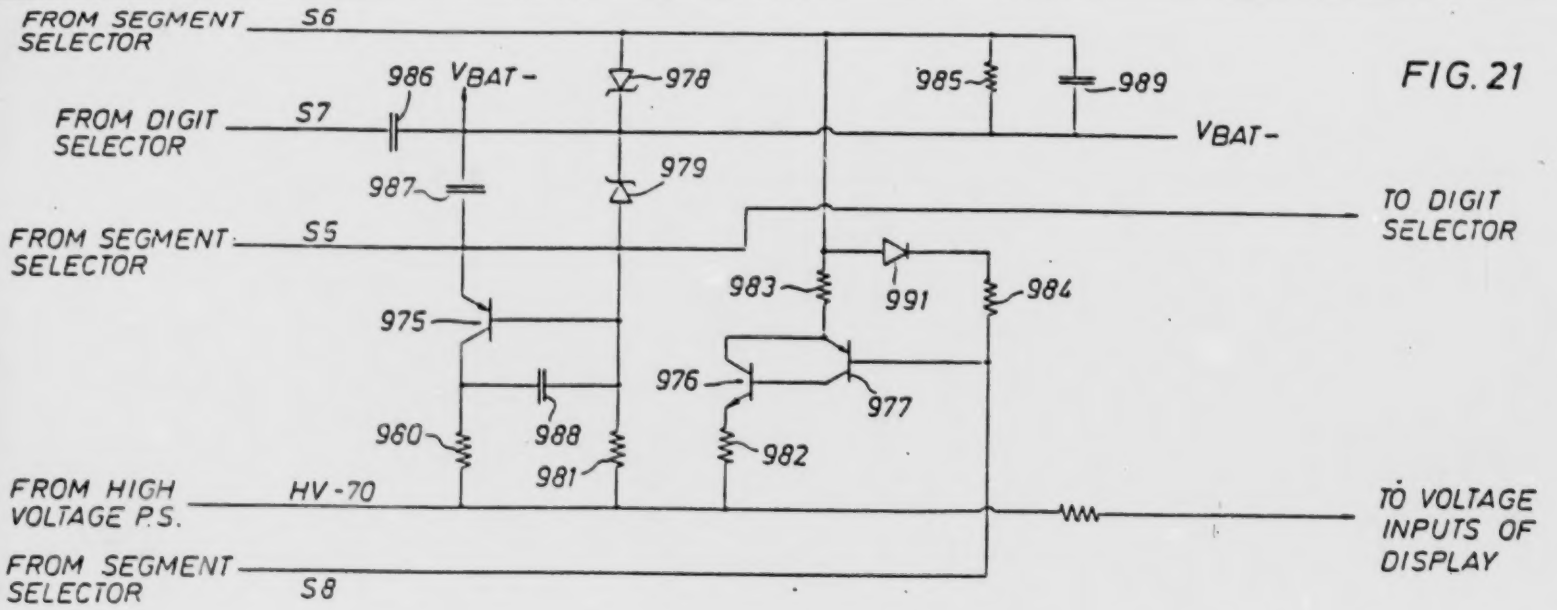

FROM SEGMENT SELECTOR
S6
986
VBAT-
978
985
989
FROM DIGIT SELECTOR
S7
VBAT-
987
979
TO DIGIT SELECTOR
FROM SEGMENT SELECTOR
S5
983
991
984
975
976
977
960
988
981
982
FROM HIGH VOLTAGE P.S.
HV-70
TO VOLTAGE INPUTS OF DISPLAY
FROM SEGMENT SELECTOR
S8

FIG. 21

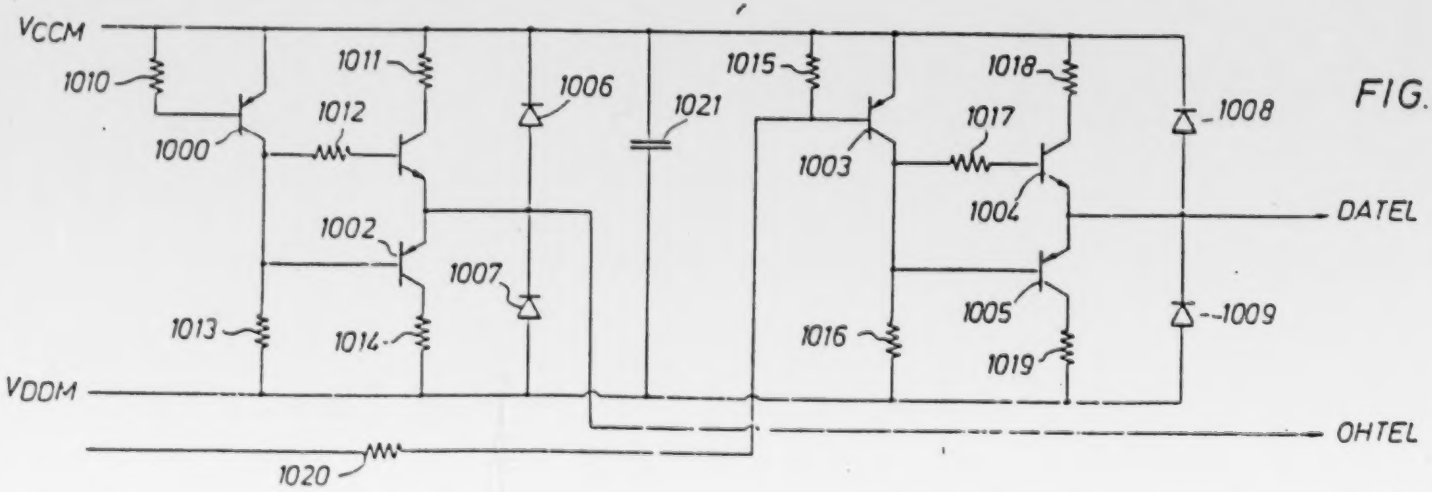

VCCM
1010
1011
1006
1015
1018
1012
1021
1017
1008
1000
1003
1004
DATEL
1002
1007
1005
1009
1013
1014
1016
1019
VDDM
OHTEL
1020

FIG. 22

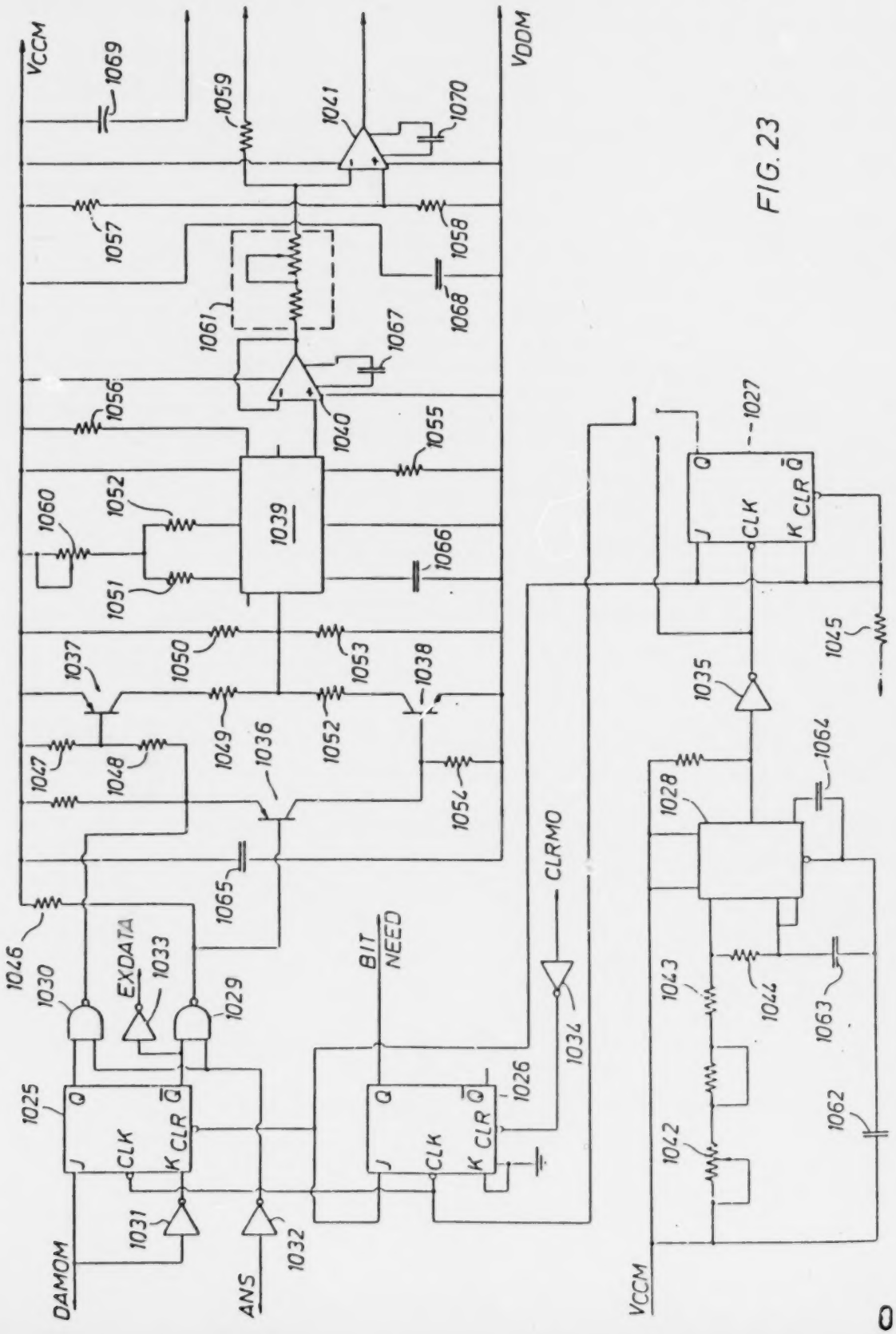

VCCM
VDDM
1069
1059
1041
1070
1057
1058
1061
1067
1068
1040
1056
1055
1060
1052
1039
1066
1051
1050
1053
1037
1038
1049
1036
1052
1047
1048
1054
1065
1046
1030
EXDATA
1033
1029
BIT NEED
CLRMO
1034
1026
1025
Q
CLK
K CLR Q̄
J
1031
1032
DAMOM
ANS
1027
1035
1045
1064
1028
1043
1044
1063
1042
1062
VCCM

FIG. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

ENT NO. : 3,956,740

TED : May 11, 1976

VENTOR(S) : Michael Dale Jones et al

It is certified that error appears in the above-identified patent and that said Letters Patent hereby corrected as shown below:

ol. 2, line 48, change "per" to --power--.
ol. 4, line 13, insert --MODE-- after "the".
ol. 4, line 43, change "drive" to --drives--.
ol. 5, line 30, delete "optical" and insert --optional--.
ol. 6, line 1, insert --modulus-- following "either".
ol. 6, line 57, delete "happening" and insert --beginning--.
ol. 8, line 3, delete "SEN" and insert --SEND--.
ol. 21, under ROM Number 6-continued, delete "Addresses 0 to 127" and substitute --Addresses 128 to 255--.
n the first printed page of the specification, add --John M. Humphreys of Dallas, Texas-- as an inventor.

Signed and Sealed this

Twenty-fourth Day of August 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks

PORTABLE DATA ENTRY APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to improvements in portable data devices of the type wherein data may be keyed, viewed for accuracy, recorded on magnetic tape, recalled from magnetic tape, and telephonically transmitted for processing.

2. Description of the Prior Art

At the present time there are various types of data collection systems in use for collecting and recording various types of data. Data that is collected by these systems is usually transmitted by conventional means to a central computer for further processing. These data collection systems are especially useful to supermarkets and drug stores as a means of ordering merchandise.

One type of data collection system developed to date generally uses a modified adding machine as an input device to a recording medium. These types of systems are usually cumbersome to use, since carts are required to transport them. Furthermore, these systems require conventional 110 volt electricity for operation, leading to awkward power cords and limited mobility.

Portable data entry devices have been developed to alleviate some of the problems associated with the above devices. These portable devices have, not, however, provided total flexibility. Moreover, they have not provided sufficient safeguards against un-noticed operator error, e.g., inadvertent deletion of data, and they have been too complicated for many users to operate correctly and consistently, especially untrained persons.

SUMMARY OF THE INVENTION

The present invention overcomes the shortcomings of the prior art without sacrificing light weight or portability.

The system provides for recording data on a tape cassette in a portable case, which also includes a microcomputer set and batteries. A hand-held keyboard input unit, including a display, is connected by a cable to the case. In one aspect of the invention, circuitry is provided for generating a signal when the battery voltage is below one predetermined level. The signal is inputted to the microcomputer set, which generates a signal sequence to the display, indicating the low-battery condition.

In another aspect of the invention, the batteries are automatically electronically disconnected when battery voltage drops below a second predetermined level. This feature is part of the "data integrity" theme of the invention.

Various components are powered and shut down as functionally required, thereby prolonging battery life.

An important aspect of the present invention is that it permits, upon operator key command, a re-winding of the tape and an automatic search for a signal pattern corresponding to a coded item chosen by the operator, or, if the operator so elects, an item-by-item scan of all previous entries. Additionally, the three previous entries at any given time are stored in memory, and may accordingly be reviewed without moving the tape at all.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a perspective view of the portable apparatus of this invention.

FIG. 1*a* is a more detailed view of the keyboard unit 90 of FIG. 1.

FIG. 2 is a block diagram illustrating the electrical arrangement of the system of this invention.

FIG. 3 is a schematic diagram of the power supply circuitry of the system of FIG. 2.

FIG. 4 is a schematic diagram of the power-switching circuitry of the system of FIG. 2.

FIG. 5 is a schematic circuit diagram of a microcomputer set of the system of FIG. 2.

FIG. 6 is a schematic diagram of clock generation circuitry of the system of FIG. 2.

FIG. 7 is a schematic diagram of the port selector circuitry of the system of FIG. 2.

FIG. 8 is a schematic diagram of the input port circuitry of the system of FIG. 2.

FIG. 9 is a schematic diagram of the output port circuitry of the system of FIG. 2.

FIG. 10 is a schematic diagram of the read-write circuitry of the system of FIG. 2.

FIG. 11 is a schematic diagram of the deck-motion-control circuitry of the system of FIG. 2.

FIG. 12 is a schematic diagram of the alarm clock circuitry of the system of FIG. 2.

FIG. 13 is a schematic diagram of the alarm circuitry of the system of FIG. 2.

FIG. 14 is a schematic diagram of the bit cell timer circuitry of the system of FIG. 2.

FIG. 15 is a schematic diagram of the emitter detector circuitry of the system of FIG. 2.

FIG. 16 is a schematic diagram of the delay circuitry of the system of FIG. 2.

FIG. 17 is a schematic diagram of the segment selector circuitry of the system of FIG. 2.

FIG. 18 is a schematic diagram of the digit selector circuitry of the system of FIG. 2.

FIG. 19 is a schematic diagram of the keyboard switch and interrogation circuitry of the system of FIG. 2.

FIG. 20 is a schematic diagram of the high voltage power supply of the system of FIG. 2.

FIG. 20*a* graphically shows the output waveform of one component of the high voltage per supply of FIG. 20.

FIG. 20*b* is a simplified schematic diagram of the high voltage power supply of FIG. 20.

FIG. 21 is a schematic diagram of the power saving circuitry that is used in conjunction with the high voltage power supply of FIG. 20.

FIG. 22 is a schematic diagram of portion of the modem circuitry of the system of FIG. 2.

FIG. 23 is a schematic diagram of the portion of the modem circuitry of the system of FIG. 2 which interfaces an acoustical coupler.

DESCRIPTION OF THE PREFERRED EMBODIMENT

It will be appreciated that the present invention can take many forms and embodiments. The true essence and spirit of this invention are defined in the appended claims, and it is not intended that the embodiment of the invention presented herein should limit the scope thereof.

ferring now to FIG. 1, the external configuration
he portable data entry apparatus of this invention is
wn. This apparatus is comprised of a keyboard in-
display unit 90, a housing 91 in which a tape deck
hanism and a majority of the electronics embody-
this invention are located and into which a mag-
c cassette tape cartridge 94 may be inserted, and
cable 92 which connects housing 91 and keyboard-
ay unit 90. A specific function, e.g., the entry of
, to be performed by the portable data entry appa-
s is selected by the operator. This is accomplished
utilization of the keyboard input-display unit 90.
electronics which reside in housing 91 detect the
tion to be performed, and, in the case of data en-
generate proper electrical signals to cause the data
e written on the tape in the tape cartridge 94. Also
electronics position the tape such that it is ready
pt new data.

ferring now to FIG. 2, there is shown a block dia-
n of the portable data entry apparatus of this inven-
It is comprised of microcomputer set 100, clock
port selector 103, input port 104, output port 105,
motion control 106, read-write circuitry 107, bit
imer 108, display 109, high voltage power supply
keyboard switch and interrogation assembly 111,
n 112, delay 113, modem 114, power supply 115,
er switching 116, alarm circuitry 117, emitter de-
r 118, segment selector 119, and digit selector
It will be appreciated that the block diagram is
ated to give a general understanding of interrela-
of the above interrelated elements. It should also
ppreciated that the detailed interconnection of the
ous devices is not given at this point for ease of
entation of the block diagram. The detailed inter-
ection of these devices will be set forth later in the
ification.

e operation of the apparatus of this invention be-
with reference to FIG. 2, by assuming that no
ious data have been recorded on tape and that the
ator is just beginning to use the apparatus. Tape
idge 94, is, therefore, inserted in the housing 91,
the power switch on. Keyboard input-display unit
engaged in the "on" position. This switch is sche-
cally shown in FIG. 19, and its being engaged on
es power supply 115 to be activated.

nce the source of power for the portable data entry
aratus of this invention is batteries, it is desirable to
imize the consumption of battery power. Power
ching unit 116 (FIG. 2) accomplishes this by sup-
ng power to certain component parts only when
er to those parts is required for proper operation.
example, power is supplied to the modem 121 only
n the operator puts the unit in the "send" mode as
ribed below, an power is supplied to the tape deck
when the operator puts the unit in either the
D or RECORD modes.

rthermore, battery power is conserved when in
r modes by switching the power to component
s by the apparatus at periodic intervals. The length
me that power is available to these components is
ed to as the "awake" time, and the length of time
it is not available is referred to as the "asleep"
In the preferred embodiment of this invention the
mum awake time is approximately 2.5 millisec-
, and the asleep time is approximately 7.5 millisec-

wer supply 115, when activated, supplies power
tly to the microcomputer set 100, and the mi-

crocomputer set 100 begins to execute a series of pre-
determined instructions, as later illustrated. Since at
this point in the operation only the power switch has
been turned on, the microcomputer set 100 is interro-
gating the keyboard switch (FIG. 19) and interrogation
circuitry 111 via the segment selector circuitry 119 to
determine if a mode has been selected by the operator.
Since no previous data has been recorded on tape and
the operator was just beginning to utilize the apparatus,
assume now that the operator desires to enter the RE-
CORD mode.

To enter the RECORD mode for a new tape the
operator must press first the ["*"] of FIG. 11 key (FIG.
19) and then must depress the CLEAR key (FIG. 19)
for approximately 5 seconds. The microcomputer set
100 first detects that the MODE key had been de-
pressed and then that the CLEAR key had been de-
pressed for the required five seconds. After five sec-
onds the microcomputer set generates commands via
the output port 105 (FIG. 2) to the deck motion con-
trol 124 to cause the tape of the cartridge 94 to be
rewound. After the tape has been rewound, the deck
motor mechanism is enabled by deck motion control
124 to start the tape moving in the forward direction
until the beginning of the tape is found. The beginning
of tape is found by utilizing emitter detector 118. The
operator is now ready to begin entry of data.

Data may be entered by depressing the appropriate
keys of the keyboard input-display unit 90 (FIG. 1)
which are shown schematically in the keyboard switch
and interrogation circuitry 111 of FIG. 19. Suppose, for
example, that the data "12345" were desired to be
written onto tape. The operator would depress the 1
switch, followed by the 2 switch, etc. until the five
switches have been depressed. The data are then dis-
played in the display unit 109.

If the operator had attempted to enter data into the
date entry apparatus prior to entering the RECORD
mode, it would not have been accepted since the appa-
ratus is in a no mode or idle status. The microcomputer
set 100 at this time generates signals to the alarm cir-
cuitry 112, and the alarm circuitry 112 detects these
signals and drive a speaker for a specified period of
time. The operator is, therefore, given an audible indi-
cation that the data apparatus is not in the proper mode
to accept data entry. The above described alarm is
present anytime that the portable data entry apparatus
is in a no mode or idle status.

In a manner to be later set forth in detail, when the
portable data entry apparatus was placed in the RE-
CORD mode, the microcomputer set 100 started scan-
ning the keyboard switch and interrogation circuitry
111 during the awake time to determine if a key has
been depressed. As each key in the above example was
depressed, it would be detected by the microcomputer
set 100 during this scan and the information corre-
sponding to that key would be detected and would be
temporarily stored in the microcomputer set 100. This
stored information is then outputted to the display 109
via the segment selector 119 and the digit selector 120
during the awake time of power switching unit 116,
thereby giving the operator a visual indication of the
entered data. In the preferred embodiment of this in-
vention up to 12 digits may be displayed for any one
entry.

A primary use of the portable data entry apparatus of
this invention is to enable merchandisers, e.g., super-
market chains, to employ it for ordering information.

Each type of goods that is to be ordered will have a reference designation symbol, and it is common for this reference designator to be five digits in length. The operator would enter the reference designator of the product to be ordered. Following this entry, he would enter the number of cases of that product to be ordered. For example, if the reference designator was 12345 and six cases were desired to be ordered, the operator's data input would be 12345064. Conversely, if in the above example only five cases need to be ordered instead of six, the operator could correct this mistake on his next entry by entering 1234501−.

When the operator of the apparatus depresses either the plus or the minus key of the keyboard 90, the microcomputer set 100 detects that fact and begins to prepare the stored information to be written onto the tape. It transmits this information in serial fashion via the output ports 105 to the read-write circuitry 107 which writes the information on the tape. The tape would then contain digitized coded signals corresponding to the data entry. Also during this write time the microcomputer set 100 has generated commands to the deck motion control 106 via the ouput ports 105 so that the tape may be properly positioned to accept the data. When the information is being written onto tape power switching unit 116 supplies power to the deck motion control 106 and the read-write circuitry 107.

At this point it is appropriate to point out that the portable data entry apparatus of this invention has several optical features. These include case total, auto header, and check digit verification. Check digit verification and case total are features which may be manually disabled, and auto header, if selected, becomes a permanent feature of the portable data entry apparatus.

If the auto header feature is selected, a command will be generated by microcomputer set 100 to write a reference designator and a number designator as the first entry on tape. This occurs when the beginning of tape is found by the emitter detector 118 as described above. In the preferred embodiment of this invention, the auto header reference designator is "ACEO", and the number designator is comprised of four numbers, e.g., 1234. The reference designator is permanently stored in microcomputer set 100 and the number designator (corresponding to unit serial number), is diode programmed (944*a* — FIG. 19) by inserting diodes corresponding to the binary coded decimal representation of the serial number. The reference designator and the number designator are always written onto the tape as the first entry if the option is installed.

The case total option is selected by engaging the case total switch of keyboard input-display unit 90 into the on position. This switch is shown schematically in FIG. 19. The microcomputer set 100 detects that this option has been selected and for all the data entries keeps a running total of the number of cases of merchandise that have been ordered. This information is usable to the operator for freight and shipping information, because from case total he can estimate how many trucks are required to transport the total order to his location. The case total switch must be engaged in the on position during the entire time the data entry is being made in order to have an accurate case total.

Check digit verification is enabled by engaging the check digit verification switch on the keyboard input-display unit 90. This switch is shown schematically in FIG. 19. When engaged, the microcomputer set 100 manipulates entered data by either 10 (double-add-double) or modulus 11 (IBM standard) check digit schemes, which are known to those skilled in the art. The data entry must be 5, 6, 7, or 8 digits for check digit verification to operate properly.

Another feature of the microcomputer set 100 is that it is capable of storing the three data entries previous to the data entry in progress. When the operator is in the record mode, the last entry on tape may be reviewed by depressing the scan key once, the second to last entry may be reviewed by depressing the scan key a second time, and the third from last entry may be displayed by depressing the scan key a third time. A fourth depression of the scan returns the operator to his entry in process, and if he had not selected an entry, the display entry wil be blank. When the operator depresses the "plus" or "minus" key for the present entry, the data entry that was previously third entry back is no longer stored in the microcomputer set 100.

Another feature of the portable data entry apparatus of this invention is the end-of-data mark which is written onto the tape whenever the operator exits the record mode. The microcomputer set 100, upon detection of a mode change, automatically generates the sequence of bit signals to the read-write circuitry 107 via the output port 105. In the preferred embodiment of this invention, this entry would be displayed as "END".

Having entered data on the tape, the operator may now desire to enter the READ mode. This may be accomplished by depressing the MODE key (FIG. 19) followed by the READ key (FIG. 19). When entering the READ mode from the RECORD mode, the display will show END. This is because the next entry on tape is the end of data mark as discussed above. When END is displayed, the portable data entry apparatus reverts to a no mode or idle status. At this time the microcomputer set 100 will generate a signal to the alarm circuitry 112 via the output ports 100. This signal will be used by the alarm circuitry 112 to drive a speaker, thereby informing the operator that a mode request needs to be made.

An alternative method of entering the READ mode is to depress the MODE key (FIG. 19) followed by the BACK key (FIG. 19). If the "MODE" and the "BACK" keys are depressed when in the RECORD mode, the portable data entry apparatus will back up and display the 10th entry back. This operation can be executed at any point on the tape. The apparatus displays the 10th entry back, and then automatically enters the read mode.

Yet another method of entering the READ mode is to depress the MODE key followed by the RWD key (FIG. 19). The microcomputer set 100 (FIG. 2) detects the depression of the MODE and RWD keys and generates signals to the deck motion control 106 which cause the tape to be rewound. The happening of tape is then found with the emitter detector 118, and data may be read from the tape.

After the read mode has been entered the operator has two methods for scanning or reviewing the data. He can "SCAN" his data by successively displaying each entry, or he can "SEARCH" for a particular entry or series of entries on tape.

If the operator desires to scan the data, he does so by depressing the scan key when in the READ mode. The entry at a given tape position is then displayed until the scan key is again depressed, at which time the next

061

y is displayed. This process can be repeated until end of data is reached at which time END is dis-ed

on the other hand, the operator desires to search particular entry or series of entries he may initiate arch request. This is accomplished by depressing a key when in the READ mode. The microcomputer 00 detects the depression automatically as an in-ion to do a search operation. The operator would enter a mask into the display. The mask is the ence designator of the type of entry that he desires splay. For example, if he desired to know the num-of cases of goods of type 12345 that had been red, he would enter the mask 12345. The search ne is enabled by then depressing the SCAN key 19) after the entry of the mask. Read-write cir-y 107 then begins to read the information that is ded on tape in a forward direction from the point he tape where the search is initiated. The informa-that is read is presented to microcomputer set 100 he bit cell timer 108 and the input ports 104.

hen a match is made, the portable data entry appa-will terminate the search and display the com-entry from tape. A match is made when each acter in the mask compares to each character of eference designator in the entry for as many char-s as were entered in the mask. If the scan key is essed again after the first match was found, the h operation will continue with the previous mask, by locating all entries on the tape with that refer-designators. To change the mask after a match, perator must depress the "CLEAR" key and then a mask and depress the SCAN key again. If, how-he desires to review entries one at a time after a h, the operator depresses the CLEAR key fol-d by the SCAN key.

will be recalled from the above description of the ORD mode that the entry into the RECORD mode only described for a tape which contained no data. e case that an operator desires to enter data onto e on which there is previously recorded data and e case of returning to the RECORD mode after a h has been completed, the RECORD mode is ed by depressing first the MODE and then the ORD keys. The microcomputer set 100 in its key-d scan detects that these two keys have been de-ed and generates signals to the deck motion con-106 to start the tape moving in the forward direc-until the end of data mark is found. It will be re-d that any time that the portable data entry appa-exited the RECORD mode the microcomputer set enerated signals to cause an end of data mark to itten onto the tape. During the time that the tape ving in the forward direction, information is being from the tape by read-write circuitry 107, and this mation is presented to microcomputer set 100 via t cell timer 108 and the input ports 104. When e end of data mark is detected by the microcom-set 100, signals are generated to the deck motion ol 106 to stop the forward motion of the tape. The tor would then be at the proper place on the tape gin additional data entries.

ing completed the data entry onto tape and, if d, having reviewed the entered data, the operator now or at some convenient time desire to trans-e entered data to a central location where his would be processed. In order to transmit the mation, the operator must put the portable data entry apparatus into the SEND mode, and this is accomplished by depressing first the MODE key and then the SEN key. The microcomputer set 100 detects that the send mode has been selected and enabled the power switching unit 116 to supply power to the modem 114. When the distant receiving end is connected to the modem the microcomputer set 100 generates commands which cause the data to be read from the tape by the read-write circuitry 107. This information is presented to the modem 114, and modem 114 translates the digital information into audio tones suitable for transmission over telephone wires. When the end of data mark is found on the tape the transmission is complete and the microcomputer set 100 generates signals which cause the tape to be rewound and then moved to the beginning of tape position. The portable data entry system is then ready to retransmit the data if required, and the display 109 will display the symbol "POLL", which indicates to the operator that the data has been transmitted.

Having now set forth the functional interrelationship of the component parts of an embodiment of this invention, it is now appropriate to describe details of the structure which accomplishes the above enumerated functions. Interconnections between the various components will be indicated in the drawings.

In the detailed description of the circuitry, the values of resistance and potentiometers are given in ohms, and, unless otherwise noted these values have a tolerance factor of ± 5% and a power rating of one-quarter watt. The symbols "K" and "M" are used for one thousand and one million, respectively. Unless otherwise noted, values of capacitance less than 1000 pfd will have a tolerance factor of ± 10%, values of capacitance greater than 1000 pfd will have a tolerance factor of + 80%, − 20% and the working DC voltage rating of the capacitor will be 20 volts. The identification of transistors and diodes is given in their EIA-registration number wherever possible. Transistors and diodes not having EIA-registered numbers, and operational amplifiers are identified by a Motorola Semiconductor Products, Inc. designation known to persons skilled in the art. The circuitry of this invention also utilizes digital integrated circuits to perform certain functions. The integrated circuits utilized are from the series 54LS/74LS, and the series 54C/74C, and identification of components is made by utilizing these designators. These series and the individual integrated circuits are described in "The TTL Book for Design Engineers," published by Texas Instruments, Inc. (1973).

Referring now to FIG. 3, there is shown a schematic diagram of power supply 115 which is utilized in the preferred embodiment of this invention. The circuitry is comprised of potentiometers 125 through 127, resistors 192 and 128 through 160, capacitors 193 and 161 through 172, transistors 173 through 183, diodes 194 and 181 through 185, operational amplifiers 186 through 189, voltage regulator 190, and inductor 191, all connected as shown. Transistor 177 is mounted on heatsink 195.

The function of power supply 115 is to supply power to the apparatus, and it derives its source of power from high quality nickel cadmium batteries. As used in the claims, the term "battery" should be understood to include either a single cell or a plurality of cells, connected in either series or parallel, to achieve the desire volt-amp rating required for proper operation of the portable data entry apparatus. The positive and nega-

tive sides of the battery are connected to the points v_{bat} and v_{bat} respectively. Signal POWSW becomes active the power is turned on and causes voltage regulator 190 to be turned on. One of the outputs of the voltage regulator 190 is a signal designated as GND. This signal is ground for the system, and when present, provides a flow path for current from v_{rrr} and v_{ddd} to the respective components of the portable data entry apparatus.

Since batteries provide the source of power for the apparatus of this invention, it is desirable for the operator of this apparatus to know when the battery power is becoming low. This can be accomplished by the circuitry of power supply 115 by adjusting 125 until the voltage at the positive input to operational amplifier 188 is equal to 2.4 volts with a battery potential of 17 volts. When the battery potential difference is less than 17 volts (i.e., through use has decreased to 17 volts) the outputs of operational amplifier 188 will become active, thereby turning off transistor 180. The signal LOWBATT will then be active and inform the microcomputer set 100 (FIG. 5) of the low battery condition. Due to the programming of the microcomputer as hereinafter set forth, when the LOWBATT signal is received by the microcomputer, it proceeds to inform the operator of the low battery condition by generating appropriate signals to the digit selector 120 and to the segment selector 119. These in turn activate the display 109 with a suitable pattern, e.g., "LO." The microcomputer set 100 also commands an end of data mark to be written on the tape to insure proper termination of the data record and generates signals to the deck motion control 106 to cause the tape to be rewound approximately sixteen entries.

When the potential difference across the batteries is less than 15.5 volts the output of operational amplifier 187 becomes active, thereby causing an electronic shut down of the unit by electronically disconnecting the batteries by removing substantially all the load from the batteries. This electronic shut down protects the batteries and prevents cell reversal. Cell reversal requires replacement of the batteries, since they can no longer be recharged. The electronic shut down feature of the apparatus of this invention protects, therefore, the user's investment in the batteries.

In the preferred embodiment of this invention the values of types of the various components of FIG. 3 are:

Potentiometer 125 has a maximum resistance of 10K, potentiometer 126 has a maximum resistance of 6K, and potentiometer 127 has a maximum resistance of 4K.

The values and types of the other components utilized in FIG. 3 are:

resistors 128, 130, 132, 133, 134, and 136: 20K;
resistor 129:110K;
resistor 131:75K;
resistor 135:120K;
resistors 137, 142, 156, and 158:10K;
resistors 138, 151, and 152:3.9K;
resistor 139:2.49 K, 1%, 1 watt;
resistors 140 and 153:24K;
resistor 141:10M;
resistor 143:47K;
resistor 144:1K;
resistor 145:220;
resistor 146:200;
resistor 147:100;
resistors 148 and 150, and 192:27K;
resistor 149:2K;
resistors 154 and 157:150K;
resistor 155:2.4K;
resistors 159 and 160:470;
capacitors 161 and 162:47mfd,
capacitor 163:100pfd;
capacitor 164, 168, 169 and 172:.1mfd,
capacitor 193:0.25mfd;
capacitor 165:0.01mfd;
capacitor 166:33pfd;
capacitor 167:47mfd;
capacitors 170 and 171:0.001mfd,
transistor 173:MPS 3707;
transistors 174, 175, and 180:2N4125;
transistor 176:MPS 404;
transistor 177 and 178:MJE 200;
transistor 179:MPS 5172;
diodes 181, 182, 184, and 185 and 195:1N914;
diode 183:UCD329;
operational amplifier 186,197, and 188:MC3302
operational amplifier 189:LM301 (National Semiconductor Corp);
voltage regulator 190:LM304 (National Semiconductor Corp);
inductor 191:1 millihenry.

Referring now to FIG. 4, there is shown the detailed schematic diagram of the proper switching unit 116 which is utilized in the preferred embodiment of this invention. It is comprised of resistors 200 through 218, inverter elements 219 through 224, transistors 225 through 232, and diodes 233 through 236, and the devices are connected as shown.

Since the source of power for the portable data entry apparatus of this invention is batteries, it is desirable to prolong the length of time that useful battery power is available. Power switching unit 116 accomplishes this by supplying power to certain component parts only when power to those parts is required for proper operations. For example, power is supplied to the modem 121 only when the unit is in the SEND mode and the tape is moving, and power is supplied to the tape deck only when the tape is to be moved.

Furthermore, battery power is conserved in the portable data entry apparatus by switching the power (V_{rrr} and V_{ddd}) to certain component parts of the apparatus of periodic intervals. The length of time that v_{rrr} and v_{ddd} are active is referred to as the "awake" time and the length of time that v_{rrr} and v_{ddd} are inactive is referred to as the asleep time. In the preferred embodiment of this invention the maximum awake time is approximately 2.5 milliseconds, and the asleep time is approximately 7.5 milliseconds.

In the preferred embodiment of the portable data entry apparatus of this invention, the values and types of the components utilized in the power switching unit 116 are:

resistors 200 and 201:6.2K;
resistor 202:20K;
resistors 203, 205, 207, and 209:4.7K;
resistors 204, 206, 208, 210, 212, 213, 216 and 218:1K;
resistors 211 and 217:2.4K;
resistors 214 and 215:3.6K;
transistors 225 and 228:2N4403;
transistors 226 and 229:2N4125;
transistors 227, and 233, and 230:2N4401;
transistor 231:MJE210;
transistor 232:MPS5172;

ters elements 219 through 224:74L04; and
s 234 through 237:1N914.

ferring now to FIG. 5, there is shown a portion of
icrocomputer set 100 that is utilized in the pre-
l embodiment of this invention. It is comprised of
tral processing unit (CPU) 300, a random access
ory (RAM) 301, a standard memory interface set
rised of devices 302 and 305, read-only-memories
1) 303 and 304, decoder 306, diode 307 and 308,
ors 309, 310, and 311, diodes 312, inverter ele-
313, capacitors 314 through 316, and trasistors
nd 318, and the devices are connected as shown.
tral processing unit 300, RAM 301, the standard
ory interface set comprised of devices 302 and
and ROM's 303 and 304 comprise a MCS-4 mi-
mputer set which is vended by Intel Corp. of
Clara, California. Its operation is described in
Users Manual of February 1974. For ease of pre-
ion only two ROM's 303 and 304 are shown in
5, but in the preferred embodiment of this inven-
seven ROM's are utilized in the microcomputer
00. The ROM's not shown are connected in the
fashion as the two ROM's that are shown.
discussed in the Intel Corp. Users Manual for the
computer set, CPU 300 is preferably an Intel
RAM 301 is preferably an Intel 4002-1, device
s preferably an Intel 4008, device 305 is prefer-
ably an Intel 4009, and the ROM's are preferably Intel 1702A's.

Decoder 306 is a 74L42, and it is utilized to decode the binary values assumed by the control lines which are outputs of device 302. The output corresponding to the decoded input is used to select a particular ROM which is to be accessed. Therefore, since seven ROM's are used in the preferred embodiment of this invention, seven output lines (binary values 0-6) of decoder 306 are utilized to select the appropriate ROM. Resistors 309 are pullup resistors for the outputs of the ROM's, and in the preferred embodiment of this invention are 20K in value.

The contents of each address of each ROM are programmed to contain a particular bit configuration. When a ROM is addressed by the CPU 300, this bit configuration is available at the output of the ROM for use by the CPU 300. The particular bit configuration is, of course, dependent upon the function that is to be performed. The preferred programming of the contents of each address of each ROM is given below. Each ROM contains 256 addresses, and the contents of each address is given in the decimal equivalent of its binary value. Those skilled in the art will realize that in order to program the ROM, a conversion from decimal to binary must be accomplished.

ROM Number 1

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
0	216	32	161	64	231	96	37
1	81	33	46	65	216	97	20
2	72	34	48	66	228	98	112
3	84	35	47	67	82	99	242
4	23	36	228	68	189	100	28
5	81	37	220	69	26	101	106
6	77	38	81	70	73	102	81
7	32	39	72	71	82	103	72
8	48	40	85	72	163	104	64
9	33	41	209	73	82	105	104
10	236	42	68	74	219	106	82
11	177	43	229	75	46	107	36
12	85	44	65	76	13	108	20
13	23	45	49	77	47	109	37
14	33	46	67	78	224	110	66
15	48	47	223	79	126	111	74
16	49	48	17	80	77	112	237
17	28	49	60	81	81	113	177
18	245	50	27	82	252	114	208
19	82	51	142	83	20	115	229
20	36	52	140	84	89	116	64
21	20	53	44	85	81	117	30
22	37	54	213	86	64	118	216
23	18	55	46	87	64	119	228
24	30	56	138	88	245	120	84
25	68	57	241	89	214	121	235
26	231	58	97	90	143	122	209
27	84	59	118	91	26	123	226
28	235	60	28	92	81	124	82
29	177	61	245	93	85	125	163
30	85	62	230	94	209	126	82
31	173	63	209	95	64	127	245

ROM Number 1

Addresses 128 to 255

Address	Value	Address	Value	Address	Value	Address	Value
128	85	160	227	192	168	224	82
129	156	161	46	193	246	225	137
130	46	162	255	194	246	226	64
131	93	163	47	195	18	227	93
132	82	164	227	196	209	228	113
133	196	165	82	197	33	229	153
134	26	166	219	198	233	230	85
135	209	167	81	199	96	231	178
136	70	168	252	200	33	232	64
137	130	169	28	201	232	233	37
138	69	170	85	202	28	234	0
139	37	171	218	203	167	235	82
140	65	172	143	204	176	236	36
141	17	173	18	205	241	237	18
142	28	174	40	206	97	238	30
143	245	175	43	207	127	239	68
144	230	176	209	208	197	240	60

ROM Number 1-continued

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
145	214	177	231	209	81	241	20
146	228	178	32	210	64	242	235
147	85	179	12	211	64	243	213
148	178	180	33	212	0	244	229
149	82	181	208	213	28	245	46
150	189	182	224	214	245	246	44
151	26	183	97	215	82	247	82
152	157	184	33	216	36	248	196
153	84	185	177	217	20	249	26
154	235	186	233	218	37	250	253
155	82	187	20	219	18	251	65
156	163	188	209	220	30	252	7
157	46	189	234	221	242	253	44
158	128	190	242	222	28	254	64
159	47	191	191	223	228	255	85

ROM Number 2

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
0	211	32	37	64	212	96	175
1	26	33	233	65	83	97	245
2	5	34	186	66	218	98	245
3	84	35	185	67	82	99	179
4	235	36	164	68	235	100	247
5	82	37	183	69	83	101	178
6	203	38	182	70	218	102	171
7	46	39	35	71	216	103	20
8	86	40	224	72	46	104	165
9	210	41	164	73	0	105	246
10	85	42	248	74	47	106	99
11	3	43	180	75	225	107	26
12	83	44	99	76	192	108	105
13	245	45	123	77	32	109	187
14	218	46	32	78	11	110	33
15	64	47	64	79	181	111	241
16	33	48	37	80	240	112	237
17	208	49	217	81	183	113	147
18	228	50	228	82	46	114	28
19	85	51	44	83	255	115	121
20	17	52	50	84	44	116	236
21	9	53	46	85	253	117	146
22	217	54	16	86	111	118	246
23	224	55	212	87	47	119	18
24	36	56	85	88	227	120	133
25	63	57	3	89	45	121	241
26	38	58	84	90	227	122	239
27	238	59	235	91	33	123	147
28	40	60	82	92	234	124	28
29	238	61	163	93	20	125	152
30	42	62	64	94	165	126	238
31	231	63	209	95	187	127	146

ROM Number 2

Addresses 128 to 255

Address	Value	Address	Value	Address	Value	Address	Value
128	246	160	241	192	235	224	203
129	26	161	20	193	81	225	214
130	152	162	102	194	233	226	184
131	238	163	67	195	117	227	250
132	16	164	245	196	220	228	125
133	236	165	113	197	35	229	208
134	184	166	86	198	233	230	0
135	219	167	33	199	36	231	0
136	136	168	164	200	203	232	0
137	18	169	228	201	115	233	0
138	154	170	165	202	204	234	0
139	185	171	229	203	171	235	0
140	209	172	166	204	246	236	0
141	186	173	230	205	187	237	211
142	43	174	167	206	26	238	190
143	236	175	231	207	246	239	241
144	20	176	192	208	81	240	216
145	150	177	36	209	232	241	136
146	208	178	15	210	82	242	184
147	228	179	40	211	194	243	47
148	105	180	224	212	26	244	226
149	105	181	37	213	218	245	192
150	185	182	203	214	223	246	219
151	16	183	226	215	182	247	190
152	162	184	82	216	65	248	126
153	16	185	219	217	193	249	248
154	168	186	139	218	65	250	65
155	180	187	244	219	216	251	210
156	182	188	189	220	0	252	83
157	163	189	83	221	0	253	217
158	181	190	217	222	0	254	82

ROM Number 2-continued

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
159	183	191	82	223	116	255	214

ROM Number 3

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
0	46	32	25	64	18	96	193
1	64	33	25	65	97	97	246
2	47	34	68	66	246	98	161
3	216	35	229	67	114	99	20
4	226	36	46	68	78	100	113
5	36	37	8	69	46	101	18
6	15	38	47	70	16	102	116
7	40	39	236	71	47	103	245
8	1	40	241	72	223	104	114
9	42	41	143	73	229	105	108
10	59	42	26	74	83	106	28
11	83	43	49	75	245	107	69
12	32	44	228	76	64	108	244
13	20	45	176	77	37	109	177
14	11	46	237	78	18	110	240
15	139	47	66	79	81	111	229
16	20	48	56	80	207	112	193
17	32	49	238	81	209	113	248
18	168	50	143	82	129	114	226
19	246	51	26	83	18	115	192
20	246	52	115	84	74	116	248
21	18	53	230	85	242	117	32
22	25	54	176	86	242	118	187
23	83	55	239	87	20	119	28
24	59	56	248	88	74	120	74
25	101	57	177	89	217	121	83
26	221	58	110	90	129	122	245
27	181	59	47	91	26	123	112
28	37	60	237	92	74	124	126
29	224	61	178	93	242	125	193
30	69	62	160	94	177	126	46
31	23	63	246	95	250	127	15

ROM Number 3

Addresses 128 to 255

Address	Value	Address	Value	Address	Value	Address	Value
128	82	160	161	192	82	224	245
129	237	161	224	193	235	225	26
130	46	162	192	194	46	226	222
131	14	163	82	195	47	227	208
132	82	164	219	196	47	228	226
133	196	165	83	197	234	229	218
134	18	166	217	198	246	230	81
135	121	167	85	199	127	231	72
136	192	168	23	200	198	232	212
137	85	169	28	201	191	233	83
138	166	170	183	202	192	234	218
139	35	171	82	203	208	235	46
140	233	172	194	204	83	236	47
141	99	173	18	205	218	237	210
142	28	174	167	206	212	238	190
143	149	175	82	207	82	239	47
144	242	176	194	208	214	240	226
145	224	177	18	209	234	241	190
146	240	178	185	210	245	242	212
147	35	179	85	211	26	243	190
148	224	180	23	212	209	244	47
149	35	181	20	213	208	245	190
150	211	182	175	214	46	246	216
151	235	183	64	215	32	247	226
152	18	184	245	216	47	248	226
153	69	185	46	217	226	249	0
154	233	186	43	218	192	250	0
155	179	187	66	219	216	251	25
156	233	188	237	220	82	252	251
157	242	189	218	221	214	253	127
158	224	190	81	222	234	254	237
159	35	191	72	223	245	255	192

ROM Number 4

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
0	176	32	169	64	71	96	246
1	49	33	20	65	100	97	189
2	50	34	89	66	212	98	240
3	179	35	43	67	148	99	182
4	52	36	234	68	28	100	192

ROM Number 4-continued

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
5	181	37	20	69	71	101	47
6	182	38	82	70	180	102	234
7	55	39	123	71	37	103	245
8	56	40	91	72	173	104	26
9	185	41	250	73	248	105	138
10	186	42	135	74	224	106	160
11	59	43	246	75	223	107	246
12	188	44	125	76	185	108	176
13	61	45	30	77	38	109	161
14	62	46	18	78	0	110	246
15	174	47	50	79	42	111	177
16	240	48	127	80	59	112	247
17	225	49	75	81	192	113	226
18	226	50	168	82	17	114	124
19	243	51	246	83	89	115	136
20	228	52	246	84	118	116	239
21	245	53	18	85	100	117	168
22	246	54	75	86	209	118	238
23	231	55	245	87	121	119	176
24	232	56	245	88	76	120	83
25	249	57	26	89	241	121	32
26	250	58	63	90	197	122	47
27	235	59	104	91	246	123	234
28	252	60	104	92	26	124	243
29	237	61	208	93	95	125	26
30	238	62	189	94	103	126	120
31	255	63	117	95	173	127	247

ROM Number 4

Addresses 128 to 255

Address	Value	Address	Value	Address	Value	Address	Value
128	226	160	176	192	197	224	228
129	168	161	85	193	242	225	44
130	246	162	136	194	242	226	69
131	26	163	85	195	28	227	85
132	139	164	166	196	198	228	211
133	241	165	160	197	184	229	26
134	245	166	20	198	233	230	243
135	184	167	202	199	177	231	83
136	32	168	64	200	48	232	245
137	255	169	241	201	192	233	82
138	192	170	241	202	46	234	219
139	83	171	115	203	110	235	83
140	32	172	179	204	82	236	217
141	163	173	98	205	196	237	46
142	241	174	212	206	46	238	43
143	149	175	146	207	84	239	82
144	28	176	28	208	44	240	237
145	170	177	179	209	102	241	81
146	241	178	178	210	210	242	64
147	162	179	83	211	18	243	64
148	148	180	32	212	215	244	37
149	28	181	47	213	64	245	216
150	170	182	234	214	33	246	83
151	143	183	245	215	65	247	252
152	26	184	26	216	55	248	46
153	136	185	179	217	214	249	41
154	209	186	240	218	46	250	82
155	226	187	226	219	48	251	237
156	46	188	35	220	47	252	46
157	12	189	210	221	226	253	16
158	82	190		222	192	254	47
159	237	191	18	223	211	255	226

ROM Number 5

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
0	192	32	35	64	26	96	87
1	249	33	240	65	112	97	217
2	164	34	232	66	175	98	81
3	176	35	20	67	246	99	72
4	153	36	59	68	26	100	220
5	146	37	187	69	74	101	226
6	131	38	208	70	85	102	110
7	245	39	179	71	173	103	85
8	128	40	46	72	68	104	23
9	152	41	128	73	231	105	28
10	136	42	185	74	46	106	231
11	198	43	35	75	29	107	47
12	143	44	233	76	82	108	234
13	134	45	177	77	196	109	246
14	191	46	56	78	176	110	18
15	226	47	47	79	26	111	103
16	146	48	227	80	87	112	217
17	134	49	41	81	175	113	81
18	171	50	227	82	245	114	72
19	161	51	99	83	26	115	222

ROM Number 5-continued

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
20	140	52	111	84	97	116	226
21	192	53	221	85	64	117	46
22	199	54	177	86	37	118	8
23	34	55	113	87	85	119	82
24	85	56	55	88	21	120	237
25	33	57	123	89	29	121	43
26	239	58	43	90	231	122	220
27	176	59	192	91	46	123	226
28	98	60	46	92	29	124	209
29	33	61	110	93	82	125	83
30	239	62	82	94	196	126	252
31	178	63	196	95	26	127	219

ROM Number 5

Addresses 128 to 255

Address	Value	Address	Value	Address	Value	Address	Value
128	82	160	83	192	193	224	23
129	230	161	101	193	242	225	20
130	46	162	230	194	245	226	160
131	14	163	43	195	245	227	67
132	82	164	191	196	16	228	160
133	237	165	154	197	242	229	64
134	34	166	26	198	212	230	254
135	0	167	132	199	180	231	83
136	36	168	223	200	37	232	245
137	0	169	191	201	180	233	64
138	32	170	68	202	216	234	33
139	255	171	198	203	226	235	82
140	46	172	168	204	212	236	203
141	111	173	246	205	18	237	212
142	82	174	246	206	209	238	83
143	196	175	18	207	105	239	252
144	46	176	156	208	214	240	82
145	16	177	219	209	43	241	189
146	47	178	155	210	226	242	26
147	26	179	20	211	36	243	240
148	151	180	185	212	160	244	83
149	219	181	83	213	83	245	252
150	16	182	61	214	101	246	82
151	219	183	68	215	83	247	185
152	231	184	156	216	32	248	82
153	243	185	241	217	20	249	189
154	247	186	165	218	213	250	26
155	230	187	147	219	17	251	237
156	40	188	243	220	229	252	65
157	16	189	164	221	83	253	71
158	42	190	146	222	101	254	211
159	39	191	26	223	85	255	44

ROM Number 6

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
0	3	32	246	64	37	96	242
1	46	33	26	65	82	97	230
2	33	34	36	66	133	98	131
3	180	35	206	67	210	99	18
4	209	36	192	68	129	100	97
5	85	37	32	69	20	101	85
6	174	38	0	70	75	102	178
7	179	39	28	71	232	103	81
8	164	40	144	72	242	104	64
9	224	41	82	73	26	105	115
10	244	42	36	74	63	106	142
11	242	43	20	75	46	107	226
12	180	44	63	76	79	108	83
13	188	45	18	77	82	109	245
14	189	46	144	78	196	110	85
15	190	47	242	79	26	111	209
16	191	48	20	80	83	112	85
17	35	49	65	81	86	113	166
18	224	50	46	82	76	114	177
19	99	51	63	83	46	115	209
20	116	52	47	84	77	116	230
21	13	53	239	85	82	117	84
22	192	54	248	86	196	118	254
23	38	55	18	87	26	119	34
24	80	56	58	88	91	120	15
25	39	57	211	89	85	121	44
26	234	58	231	90	250	122	1
27	245	59	113	91	81	123	223
28	18	60	63	92	177	124	99
29	31	61	85	93	85	125	35
30	200	62	178	94	166	126	224
31	246	63	84	95	238	127	125

ROM Number 6

Addresses 128 to 255

Address	Value	Address	Value	Address	Value	Address	Value

ROM Number 6-continued

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
128	124	160	224	192	43	224	17
129	81	161	126	193	227	225	248
130	177	162	159	194	40	226	250
131	221	163	127	195	4	227	234
132	179	164	159	196	41	228	20
133	82	165	192	197	240	229	224
134	185	166	34	198	187	230	127
135	35	167	60	199	234	231	224
136	224	168	35	200	245	232	46
137	226	169	238	201	245	233	11
138	85	170	231	202	241	234	234
139	209	171	178	203	246	235	28
140	64	172	192	204	241	236	232
141	32	173	208	205	246	237	126
142	64	174	34	206	137	238	234
143	0	175	32	207	185	239	127
144	85	176	35	208	192	240	234
145	173	177	231	209	44	241	125
146	161	178	85	210	79	242	218
147	248	179	166	211	82	243	46
148	20	180	35	212	219	244	63
149	61	181	224	213	82	245	82
150	213	182	99	214	214	246	237
151	145	183	35	215	213	247	241
152	28	184	224	216	83	248	65
153	119	185	192	217	218	249	64
154	65	186	40	218	45	250	85
155	19	187	137	219	216	251	186
156	46	188	42	220	226	252	147
157	12	189	255	221	46	253	184
158	208	190	41	222	59	254	162
159	47	191	227	223	47	255	186

ROM Number 7

Addresses 0 to 127

Address	Value	Address	Value	Address	Value	Address	Value
0	46	32	38	64	191	96	26
1	0	33	248	65	190	97	166
2	234	34	28	66	189	98	185
3	245	35	75	67	188	99	41
4	18	36	44	68	43	100	233
5	225	37	16	69	235	101	241
6	245	38	189	70	251	102	251
7	26	39	241	71	224	103	18
8	13	40	172	72	106	104	217
9	44	41	141	73	127	105	125
10	16	42	28	74	65	106	113
11	70	43	46	75	192	107	139
12	60	44	26	76	175	108	251
13	43	45	75	77	246	109	20
14	233	46	97	78	26	110	127
15	251	47	113	79	128	111	66
16	18	48	60	80	85	112	69
17	75	49	241	81	186	113	105
18	107	50	46	82	180	114	169
19	188	51	153	83	169	115	246
20	189	52	218	84	147	116	233
21	120	53	156	85	18	117	26
22	13	54	241	86	217	118	121
23	211	55	251	87	131	119	241
24	137	56	188	88	244	120	245
25	147	57	249	89	189	121	251
26	26	58	157	90	162	122	139
27	75	59	189	91	184	123	251
28	20	60	42	92	175	124	187
29	39	61	15	93	245	125	70
30	248	62	241	94	245	126	99
31	20	63	220	95	208	127	192

ROM Number 7

Addresses 128 to 255

Address	Value	Address	Value	Address	Value	Address	Value
128	67	160	123	192	251	224	111
129	245	161	146	193	18	225	192
130	85	162	220	194	196	226	163
131	178	163	224	195	242	227	20
132	179	164	69	196	180	228	225
133	217	165	91	197	241	229	240
134	224	166	147	198	118	230	43
135	38	167	18	199	190	231	233
136	171	168	217	200	218	232	251
137	40	169	41	201	133	233	18
138	208	170	233	202	18	234	247
139	42	171	189	203	172	235	107
140	7	172	209	204	117	236	120
141	46	173	181	205	175	237	230
142	133	174	241	206	173	238	210

ROM Number 7-continued

Addresses 0 to 127							
Address	Value	Address	Value	Address	Value	Address	Value
143	36	175	169	207	251	239	43
144	255	176	20	208	18	240	235
145	16	177	206	209	217	241	20
146	99	178	248	210	132	242	36
147	47	179	185	211	251	243	242
148	227	180	241	212	26	244	242
149	37	181	41	213	215	245	20
150	227	182	233	214	248	246	36
151	43	183	251	215	20	247	26
152	234	184	18	216	225	248	225
153	185	185	217	217	240	249	171
154	184	186	244	218	179	250	185
155	183	187	182	219	35	251	240
156	182	188	70	220	179	252	70
157	35	189	197	221	233	253	18
158	224	190	164	222	251	254	
159	111	191	133	223	26	255	

Referring now to FIG. 6, there is shown the detail matic diagram of the clock 102 which is used in the ferred embodiment of this invention. The circuitry comprised of capacitors 350, 351, 355, 356, 359, 376, and 378, crystal 354, resistors 352, 353, 358, 380, and 384, transistor 357, inverter elements 361, 365, 373, 374, 381, 382, and 385, NAND s 364 and 367 through 370, NAND gates 369 and flip flops 362, 363, 366, 371, and 372, MOS driver , and diode 383, connected as shown.

eference to the Intel Corp. User's Manual for the S-4 microcomputer set reveals that the microcom- has an instruction cycle time of 10.8 microsec- s. During this instruction cycle two clocks must h have active states eight times. These clock pules provided by the clock circuitry shown in FIG. 6.

the preferred embodiment of this invention, crys- 354 has a frequency of 5.185 MHz. This frequency ounted down by the divide by seven counter com- ed of flip-flops 362, 363, and 366. The frequency of outputs of NAND gates 369 and 370 are, therefore, -seventh of 5.185 Mhz. The inverter outputs of e NAND gates furnish the two clocks required by microcomputer set 100.

he values and types of the various enumerated com- ents should be:

acitor 350:0.01mfd;

acitor 351:10mfd;

acitors 355 and 356:68pfd;

acitor 359:33 pfd;

acitor 378:05 mfd;

acitors 375 and 376:0.001 mfd;

sistor 357:MPS 5172;

stor 352:2.2K;

stor 353:24K;

stor 358:51;

stors 379 and 380:10;

stor 384:6.2K;

ND gates 364, 367, and 368:74LS00

rter element 360, 361, 365, 373, 374, 381, and 2:74LS04;

rter element 385:74L04;

ND gates 369 and 370:74LS10;

flops 362, 363, 366, 371, and 372:74LS73;

S driver 377:MH0026CN (National Semiconduc- r Inc.); and

le 383:1N914.

eferring now to FIG. 7, there is shown a detailed matic diagram of the port selector 103 that is used he portable data entry apparatus of this invention. The circuitry is comprised of decoders 390 and 391, inverter elements 392 through 395, NOR gate 396, and diode 397 and is connected as shown.

As shown, the inputs to decoder 390 are the control signals C0, C1, and C2 from the microcomputer set 100 and the signal CPURST from the output port 105. The binary value of these inputs is decoded by decoder 390, and depending on the value of the inputs, one and only one of decoder 390's outputs will be active at any one time. The active output is used to select the appropriate output port to which the microcomputer set will output information via the input/output lines of device 305 (FIG. 5).

The inputs to decoder 391 are the control signals C1, C2, C3, and NIN from the microcomputer set. The decoder 391 decodes the binary value of these inputs, and one of the outputs NIN01, NIN23, NIN45, or NIN67 will be active depending upon the value of the input. The active output is used to select the input port from which data will be entered into device 305 via the input/output lines shown in FIG. 5.

In the preferred embodiment of the invention, the type of each element in the port selector circuitry is:

decoders 390 and 391:74L42;

inverter element 392 through 395:74L04;

NOR gate 396:74L02; and

diode 397:1N914.

Referring now to FIG. 8, there is shown the input port circuitry 104 which is utilized in the preferred embodiment of this invention. As shown it is comprised of data selectors 400 through 403. The data selectors are preferably 81L23's which are manufactured by National Semiconductor Corporation.

Referring now to FIG. 9, there is shown the output port circuitry 105 of FIG. 5 that is utilized in the portable data entry apparatus of this invention. It is comprised of storage devices 448 through 451, inverter elements 452 through 465, NAND gates 366 through 368, NOR gates 369 through 371, and resistor 372 and is connected as shown.

The data inputs to the output port 105 are the bidirectional input/output lines from devices 305 as shown in FIG. 5. One of the other input signals, ENOT0 through ENOT4 from the port selector 103, selects a storage element (448, 449, 450, and 451) into which data on the input/output lines is to be loaded. The data present at the output of the device selected has the same logical value as the input.

The types of the devices utilized in the preferred embodiment of this invention for implementation of

090

the output port 105 are:
storage devices 448 through 451:74L95;
inverting elements 452 through 465:74L04;
NAND gates 466 through 468:74L00;
NOR gates 469 through 471:74L02; and
resistor 472:4.7K.

Referring now to FIG. 10, there is shown the read-write circuitry 107 of FIG. 2 which is utilized in the preferred embodiment of this invention. The circuitry is comprised of NAND gates 500 through 503, transistors 504 through 508, resistors 509 through 535, capacitors 538 through 544, operational amplifiers 546 and 547, comparators 549 through 551, and diodes 552 through 554, all connected as shown.

The function of the circuitry shown in FIG. 10 is to write digitized information onto tape and to read digitized information from tape upon command. Data is written onto tape when the command WRITE is a logical one, and while data from the tape is always available at the output of read-write circuitry 107, it is utilized only upon command from the microcomputer set 100.

In the preferred embodiment of this invention the values and types of the components utilized in FIG. 10 are:
NAND gates 500 through 503:74L00;
transistor 504:2N4403;
transistors 505 and 506:2N4125;
transistors 507 and 508:2N5172;
resistors 509 and 510:1K;
resistor 511:3.3K;
resistors 512 through 515 and 530:2.7K;
resistor 516 and 517:10K;
resistor 518 and 519:20K;
resistor 520 and 531:3M;
resistor 521:82;
resistor 522:4.7K;
resistors 523, 525, and 527:47K;
resistors 524 and 528:91K;
resistor 526:2K;
resistor 529:2.2K;
resistor 532 and 533:15K;
resistors 534 and 535:10K;
capacitor 538:150pfd;
capacitors 539 and 540:10pfd;
capacitor 541:0.01mfd;
capacitor 542:33pfd;
capacitor 543:500pfd;
capacitor 544:0.01mfd;
operational amplifiers 546 and 547:LM301 (National Semiconductor Corp);
comparators 549 through 5551:LM339 (National Semiconductor Corp); and
diodes 552 through 554:1N914.

Referring now to FIG. 11, there is shown the schematic diagram of the deck motion control 106 which is utilized in the portable data entry apparatus of this invention. It is comprised of transistors 1100 through 1120, operational amplifiers 1125 and 1126, resistors 1131 through 1168, capacitors 1170 through 1176, diodes 1177 through 1178 and potentiometers 1179 and 1180 and is connected as shown. In the preferred embodiment of this invention the values and types of the components shown in FIG. 11 are:
transistor 1100:MPS404A;
transistor 1101:2N4125;
transistor 1102:MPS5172;
transistors 1103 and 1104:2N4410;
transistor 1105:MPS404;
transistor 1106:2N4403;
transistors 1107 and 1108:2N4125;
transistors 1109 and 1110:MPS5172;
transistor 1111:MJE200;
transistor 1112:MJE210;
transistor 1113:MJE200;
transistor 1114:MJE210;
transistor 1115:MJE200;
transistors 1116 and 1117 and 1118:2N4403;
transistors 1119 and 1122:2N4401;
operational amplifiers 1125 and 1126:LM301 (National Semiconductor);
resistor 1130:1K;
resistor 1131:2.2K;
resistor 1132:1K;
resistor 1133:22;
resistor 1134:56;
resistor 1135:430;
resistor 1136:10K;
resistors 1137 through 1140:4.7K;
resistor 1141:1K;
resistor 1142:2.7K;
resistors 1143 through 1146:4.7K;
resistors 1147–1149:2.2K;
resistors 1150 and 1151:2K;
resistors 1152 and 1153:10K;
resistors 1154 and 1155:3.3K;
resistor 1156:22;
resistor 1157 and 1158:10K;
resistor 1159:510
resistor 1160:2.2K;
resistor 1161:2.2K;
resistor 1162:247K;
resistor 1163:2.2K;
resistor 1164 and 1165:82;
resistor 1167:1K;
resistor 1168:680;
capacitor 1170:1mfd;
capacitor 1171:33pfd
capacitor 1172:0.1mfd
capacitor 1173:0.1mfd;
capacitor 1174:33pfd;
capacitors 1175 and 1176:0.47mfd; and
diodes 1176 through 1178:1N914.

Referring now to FIG. 12, there is shown the schematic diagram of the alarm clock circuitry 117 of FIG. 2 which is utilized in the preferred embodiment of this invention. It is comprised of inverter elements 600 and 607, NAND gates 608 through 610, operational amplifiers 111 through 614, resistors 615 through 633, capacitors 634 through 641, diodes 642 through 645, and flip flop 646, all connected as shown. Alarm circuitry 117 receives inputs from microcomputer set 100 (FIG. 5), and generates the signal MSLEEP which is utilized to switch between the awake and asleep times.

In the preferred embodiment of this invention, the values and types of the components utilized are:
inverter element 600 through 605:74CO4;
inverter elements 606 and 607:74L04;
NAND gates 608 through 610:74C10;
operational amplifiers 611 through 614:LM3900 (National Semiconductor Corp);
resistor 615:150K;
resistor 616, 617, 623, and 625:510K;
resistor 618:5.1 M;
resistors 619 and 627:1.5 M;
resistor 620:1M;

stor 621, 630, 631, and 633:1M;
stor 622:330K;
stor 624:5.1M;
stor 626:330K;
stor 628:10K;
stor 629:6.2K;
stor 632:10M;
acitor 634:0.05mfd;
acitor 635:0.002mfd;
acitor 637:750pfd;
acitors 638 and 639:100pfd,
acitor 640:0.001mfd,
acitor 641:100pfd,
des 642 through 645:1N914; and
flops 646:74C7.

eferring now to FIG. 13, there is shown the alarm nitry 112 which is utilized in the preferred embodiit of this invention. The signal NALM, from output 105, when active signifies an alarm condition. This al turns on transistor 752 which triggers timer 753. output of timer 753 then drives speaker 754 for a e, and this speaker can be heard by the operator of portable data entry apparatus.

the preferred embodiment of this invention the es and types of the components of the alarm cir-ry are:
sistors 750 and 751:2.7K;
ansistor 752:2N125's;
mer 753:NE555N (Signetics Corp.); and
apacitor 755:1mfd.

hould be observed that while an NE555N is the ferred type of device for timer 753, any compatible nostable multivibrator may be used in place of it.

eferring now to FIG. 14, there is shown bit cell r 108 that is used in the preferred embodiment of invention. It is comprised of flip flops 800 and 806, nters 807 and 808, decoders 809 and 810, exclusive gates 811 through 813, NAND gates 814 through , NOR gates 822 through 825, and inverter gates through 830. The function of the bit cell timer is to ermine the binary value of the information read m the magnetic tape.

the preferred embodiment of this invention the ious types of devices utilized are:
lip flops 800 through 806:74L73;
ounters 807 and 808:74L93;
ecoders 809 and 810:74L42;
clusive OR gates 811 and 812:74L86;
AND gates 814 through 821:74L00;
OR gates 822 through 825:74L02; and
verter elements 826 through 830:74L04.

While the foregoing schematic diagram illustrates the ferred exemplification of the bit cell timer, it should evident to those skilled in the art of logic design that above described circuitry could be implemented g a wide variety of devices as substitutes for those merated above. Any equivalents of the above enu-ated circuitry should, therefore, be so construed.

eferring now to FIG. 15, there is shown a schematic gram of the emitter detector 118 used in the porta-data entry apparatus of this invention. The function he emitter detector circuitry is to detect the pres-e of information upon the tape and to give an indi-on to the microcomputer set 100 via the input port uitry when the digit is detected. The emitter detec-circuitry is comprised of timers 760 and 761, tran-ors 762-764, resistors 765-773, capacitors

774-778, and diodes 779-784. The values and types of components utilized are:
timers 760 and 761:NE555N (Signetics Corp.);
transistor 762:MJE200;
transistors 763 and 764:NPS5172;
resistor 765:812;
resistor 766:1K;
resistor 767:470;
resistor 768:200K;
resistor 769:47K;
resistor 770:3M;
resistor 771:20K;
resistor 727:470;
resistor 773:150K;
capacitors 774 and 775:0.47mfd;
capacitor 776:0.002mfd;
capacitors 777 and 778:0.01mfd, and
diodes 779 through 784:1N914.

Referring now to FIG. 16, there is shown the detailed schematic diagram of the delay 113 circuitry which is utilized in the portable data entry apparatus of this invention. It is comprised of timer 850, transistors 815 through 854, resistors 855 through 864, potentiometer 865, and capacitors 866 through 868.

In the preferred embodiment of this invention the values and types of the components utilized in the delay circuitry of this invention are:
timer 850:NE555N (Signetics Corp.);
transistors 851, 852, and 854:MPS3702;
transistor 852:2N4125;
resistors 855, 856, and 863:1K;
resistors 857, 858, 862, and 864:4.7K;
resistor 859:30K;
resistor 860:10K;
resistor 861:1M;
potentiometer 865:20K (Maximum resistance);
capacitor 866:0.47mfd;
capacitor 867:0.01mfd; and
capacitor 868:0.05mfd.

Referring now to FIG. 17, there is shown the segment selector 119 that is utilized to select the appropriate segment or segments of the display 109 of FIG. 2, to be displayed. The circuitry is comprised of NAND gates 880 through 887, inverting elements 888 through 894, storage device 895, transistors 896 through 902, resistors 903 through 911, resistor packages 912 and 913, capacitors 914 through 920, and diodes 922 and is connected as shown.

During the period of time that inverter 894 is a logical one, NAND gates 880 through 886 are enabled and a logical one present on any of the input lines NDA0-NDA6 from the microcomputer set will cause the respective transistors 896 through 902 to be forward biased, and voltage v_{cc} will be present at the collector of any forward biased transistor. The collectors of transistors 896 through 902 are connected directly to the segment inputs of display 109 (FIG. 2).

During the period of time that the pulse NLDSTB is active, signals NDA0 through NDA3 are loaded into storage device 895 and appear at the outputs of storage device 895. These outputs are decoded by both the digit selector 120 and the keyboard switch and interrogation assembly 121.

Referring still to FIG. 17, the values and types of the components in the preferred embodiment of this invention are:
NAND gates 880 through 887:74L00;

inverting elements 888 through 891, 893, and 894:74L04;
inverting element 892:74C04;
storage device 895:DM185L51 (National Semiconductor Corp.);
transistors 896 through 902:2N6223;
resistors 903 through 909:1K;
resistor 911:10K;
resistor package 912:AS4504-02 (manufacturer is;
resistor package 913:AS4505-03;
capacitors 914 through 920:0.001mfd (1KV, 10%); and
diodes 922:1N914.

Referring now to FIG. 18, there is shown the digit selector 120 that is utilized in a preferred embodiment of the portable data entry apparatus of this invention. It is comprised of transistors 922 through 933, decoder 934, zener diode 935, and resistor packages 936 and 937 and is connected as shown.

The binary value of inputs S1-S4 is decoded by decoder 934. When decoding occurs, one and only one of the outputs of the decoder 934 will be active, thereby providing a forward bias for one and only one of the transistors 922 through 933. The collectors of transistors 922 through 933 are connected to the digit inputs of display 109 (FIG. 2) and are used by display to select the proper digit which is to be displayed.

In the preferred embodiment of this invention the values and types of the components utilized are:

decoder 934:DM74L154AN (National Semiconductor);
transistor 922 through 933:2N6223;
zener diodes 935:1N746; and
resistor packages 936 and 937:AS4504-04-330K

Referring now to FIG. 19, there is shown the schematic representation of the keyboard switch and interrogation assembly 111 that is utilized in a preferred embodiment of this invention. It is comprises of decoder 938, inverting elements 939 through 942, keyboard input switch unit 943, and diodes 944 and is connected as shown.

Periodically inputs S1-S4 from the segment selector will be activated. During the activation, binary values of 0-9 will be assumed by the four inputs. If one of the switches from keyboard input switch unit 943 have been depressed, that fact will be detected during the scan of binary values 0 to binary value 4. Outputs KERO0-KERO3 will be active and this value will be read by the microcomputer set 100 through the input ports.

The values and types of the components utilized in FIG. 19 are:

decoder 938:DM74L42AN (National Semiconductor Corp.);
inverters 939 through 942:74L04;
keyboard input switch 943:
diodes 944:1N914; and
resistors 945:10K.

Referring now to FIG. 20, there is shown the high voltage power supply 110 of FIG. 2 which is utilized in the preferred embodiment of this invention. It is comprised of NAND gates 950 through 953, transistor 954 through 956, resistors 957 through 964, capacitors 965 through 967, diodes 968 through 970, inductor 971, and capacitor 990, all connected as shown. The function of this circuitry is to convert the battery voltage to a high voltage which can be utilized by a display of the gas discharge or plasma type such as display 109 of FIG. 2. Power supply 110 functions, therefore, as a power converter.

FIG. 20*b* is a simplified schematic diagram of the high voltage supply 110 which is shown in FIG. 20. It is basically a four terminal device which has four output contact points 2000, 2001, 2002, and 2003. A d-c voltage source is connected between the first contact point 2000 and the third contact point 2002. Inductor 971 is connected between second contact point 2001 and third contact point 2002. Capacitor 990 is connected between third contact point 2002 and fourth (output) contact point 2003. A diode 2004 is connected between second contact point 2001 and fourth (output) point 2003, with the cathode of diode 2004 connected to second contact point 2001. A switch 2005 is connected between first contact point 2000 and second contact point 2001. The switch 2005 of FIG. 20*b* is comprised of transistors 955 and 956 of FIG. 20. Oscillator 2007 periodically closes switch 2005, and it is comprised of NAND gates 950 through 953, resistors 958 through 961, and capacitor 965 in FIG. 20. The sensing circuit 2006 is connected between fourth (output) contact point 2003 and oscillator 2007.

When D-C power is supplied to the portable data entry apparatus, oscillator 2007 periodically closes the switch 2005 (on time — FIG. 20*a*), and energy storage begins in inductor 971. When switch 2005 is open ("off" time — FIG. 20*a*), current flows through the loop comprised of inductor 971, capacitor 990, and diode 2004. Diode 2004 operates, therefore, as a free wheeling or flyback diode. In the preferred embodiment of this invention, the duty cycle of the output of the oscillator 2007, i.e., the ratio of the off time to the on time shown in FIG. 20*b*, is equal to the ratio of the input voltage to the output voltage and is adjusted for efficiency. During the time switch 2005 is open, current is extracted from capacitor 990 by inductor 971. The voltage at fourth (output) contact 2003 begins to increase negatively during openings of switch 2005. If this voltage were not controlled, it would approach −400 volts in value.

Sensing circuit 2006 operates as a control device for the voltage at the fourth (output) contact point 2003 and prevents the voltage at that point from significantly going more negatively than −170 volts. Sensing circuit 2006 is comprised of resistors 957 and 964, capacitor 966, and transistor 954 in FIG. 20. When the signal at fourth (output) contact point 2003 reaches approximately −170 volts, sensing circuit 2006 detects this voltage. It then inhibits oscillator 2007 from making further closures of switch 2005 until the output voltage HV−170 becomes sufficiently more positive than −170 volts. Sensing circuit 2006 detects this rise in output voltage and enables oscillator 2007. Sensing circuit 2006 functions, therefore, to stop power conversions by the power supply 110 when the output voltage is significantly more negative than −170 volts and to permit power conversion when the output voltage is significantly more positive than −170 volts. The signal HV−170 (FIG. 20) is presented to display unit 109 (FIG. 2), and it is the voltage that is used to activate display 109 when a character is to be displayed.

The various types and values of the components in the preferred embodiment of FIG. 20 are:

NAND gates 950 through 953:74L03;
transistor 954:2N4125;
transistor 955:MPSA92;
transistor 956:MPSA42;

istor 957:270K;
istor 958:2K;
istors 959 and 960:20K
istor 961:2.2K;
istor 962:680;
istor 963:68;
istor 964:10M;
pacitor 965:0.01mfd;
pacitor 966:150pfd,
istor 967:0.47mfd;
ides 968-970:1N914;
uctor 971:5 millihenrys; and
pacitor 990:0.1mfd (200v).

Referring now to FIG. 21, there is shown the circuitry t is utilized in conjunction with the high voltage wer supply 110 in the preferred embodiment of this ention. It is comprised of transistors 975 through 7, zener diodes 978 and 979, capacitors 986 through 9, and diode 991, all connected as shown.

The function of the power-saving circuitry of FIG. 21 o maintain appropriate voltages on display 109 for imum display performance.

The values and types of the components of the wersaving circuitry of FIG. 21 are:

nsistors 975 and 977:2N4888;
nsistor 976:MPSA42;
er diode 978:1N5275;
er diode 979:1N5257;
istor 980:39K;
istor 981:3.9M;
istor 982:2K;
istor 983:1K;
istor 984:20K;
istor 985:10M;
pacitor 986:0.47 mfd;
pacitor 987:1mfd (WDCV=50v);
pacitor 988:150pfd (WDCV=1000);
pacitors 989:0.1mfd (WDCV=200); and
de 991:1N914.

Referring now to FIG. 22, there is shown a portion of modem circuitry 114 that is utilized in the portable a entry apparatus of this invention. It is comprised ansistors 1000 through 1005, diodes 1006 through 9, resistors 1010 through 1020, and capacitor 1. This circuitry is utilized to interface with a Data ess Arrangement.

The values and types of the components utilized in portion of the modem circuitry 114 are:

ansistors 1000, 1002, 1003 and 1005:MPS3702;
ansistors 1001 and 1004: MPS5172;
odes 1006 through 1009:1N914;
sistors 1010, 1013, 1016, and 1020:4.7K;
sistors 1011 and 1018:62;
sistors 1012 and 1017:1K;
sistors 1014 and 1019:220; and
pacitor 1021:0.04mfd.

Referring now to FIG. 23, there is shown another ion of the modem circuitry 114 that it utilized in preferred embodiment of this invention. It is com- d of flip flops 1025 through 1027, timer 1028 ND gates 1029 and 1030, inverter elements 1031 gh 1035, transistors 1036 through 1038, voltage rolled oscillator 1039, operational amplifiers 1040 1041, potentiometers 1042, 1060, and 1061, ca- ors 1062 through 1070, and resistors 1043 gh 1059, all of which are connected as shown in Figure.

The values and types of the components utilized in this portion of the modem circuitry 114 are:

flip flops 1025 through 1027:74L73;
timer 1028:NE555 (Signetics Corp);
NAND gates 1029 and 1030:74L00;
inverter elements 1031 through 1035:74L04;
transistor 1036:2N4125;
transistor 1037:MPS404;
transistor 1038:MPS3707;
voltage controlled oscillator 1039:8038EC (Intersil Corp);
operational amplifiers 1040 and 1041:LM1301 (National Semiconductor Corp.);
potentiometer 1042:20K (maximum resistance);
resistor 1043:220K;
resistor 1044:15K;
resistor 1045:22K;
resistor 1046:1K;
resistor 1047:1K;
resistor 1048:30K;
resistor 1049:3.92K (1% metal film);
resistor 1050:3.74K (1% metal film);
resistor 1052:26.7K (1% metal film);
resistor 1052:127.0K (1% metal film);
resistor 1053:14.7k (1% metal film);
resistor 1054:1K;
resistor 1055:82K;
resistor 1056:27K;
resistors 1057 and 1058:1k;
resistors 1059:510;
potentiometer 1060:4002-P-1-402 (4K maximum rating);
potentiometer 1061:4002-P-163 (maximum rating 8K);
capacitor 1062:0.05mfd;
capacitor 1063:4700pfd;
capacitor 1064:0.01mfd;
capacitor 1065:0.05mfd;
capacitor 1066:4700pfd;
capacitors 1067 and 1070:100pfd;
capacitors 1068:0.05mfd; and
capacitor 1069:200mfd.

What is claimed is:

1. In a battery-powered portable data entry system including a keyboard unit, a microcomputer set for generating entry signals responsive to depression of keys of said keyboard unit, and recording means connected to the output of said set, the improvement comprising:

a. a tape connected to said recording means, for storing digitized coded entry signals;

b. operator-actuable means including said keyboard for searching said tape to automatically determine the presence of a selected coded entry signal; and

c. operator-actuable means for automatically positioning said tape, after said search function, at the last recorded entry signal on said tape.

2. The apparatus of claim 1, further comprising a display for receiving signals from the microcomputer set, indicative of said presence of said selected coded entry signal on said tape.

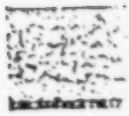
3. The apparatus of claim 1, further comprising means for displaying characters selected by the operator and identifying said selected coded entry signal and for receiving signals indicative of the presence of said selected coded entry signal on said tape.

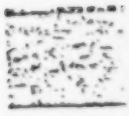
4. The apparatus of claim 1:

a. wherein said microcomputer set includes a random access memory for storing at least one prior entry signal; and

b. further comprising means for displaying said prior entry signal.

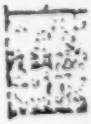
* * * * *













United States Patent [19]

Azure

[11] 4,016,542

[45] Apr. 5, 1977

[54] **ELECTRONIC NOTEBOOK FOR USE IN DATA GATHERING, FORMATTING AND TRANSMITTING SYSTEM**

[75] Inventor: Leo L. Azure, Richland, Wash.

[73] Assignee: Azurdata, Inc., Richland, Wash.

[22] Filed: Apr. 23, 1974

[21] Appl. No.: 463,400

[52] U.S. Cl. 340/172.5

[51] Int. Cl.[2] G06F 3/14; G06F 17/06

[58] Field of Search ..... 340/172.5, 173 R, 173 RC, 340/174 A, 174.1 P, 174.1 R, 347 AD, 347 DA, 324; 445/1

[56] References Cited

UNITED STATES PATENTS

3,569,940	3/1971	McFadden et al.	340/172.5
3,571,802	3/1971	Serra	340/172.5
3,593,313	7/1971	Tomaszewski et al.	340/172.5
3,678,483	7/1972	Bartocci	340/172.5
3,733,588	5/1973	Conn	340/172.5
3,760,375	9/1973	Irwin et al.	340/172.5
3,778,778	12/1973	Ragen	340/172.5
3,781,816	12/1973	Coleman et al.	340/172.5
3,781,820	12/1973	Cochran et al.	340/172.5
3,810,101	5/1974	Avery	340/172.5
3,810,107	5/1974	Goldman	340/172.5
3,859,635	1/1975	Watson et al.	340/172.5

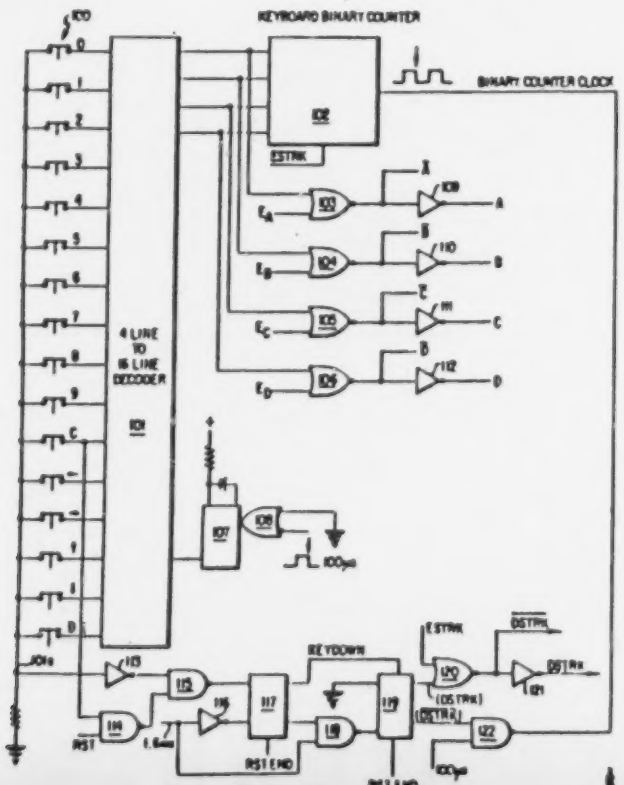
Primary Examiner—Mark E. Nusbaum

Attorney, Agent, or Firm—Staas & Halsey

[57] **ABSTRACT**

A data gathering and transmitting system includes a portable data gathering device having a keyboard and an input/output connector, each operable for entering data into, and for providing access to data previously entered into, a random access memory. Data as entered is displayed simultaneously; data in memory may be selectively accessed for display by addressed locations and in various automatic scan modes. The portable device thus operates as a true electronic notebook. An interface-formatter located at a remote terminal communicates with a computer, and provides for read-out of data from the portable data gathering device and automatic conversion and formatting of the data to a form suitable for direct transmission to the computer, and for print-out of a hard copy of the data. Where a hard copy print-out is not required, a read-out unit may simply transmit the data without formatting to a distant central receiver suitably programmed to receive and interpret the data transmission. Data may also be transmitted from a computer or distant central transmitter to the interface-formatter for entering data into the memory of the electronic notebook via the input-output connector. Thus, data can be loaded into the electronic notebook from a remote computer, the data can be displayed for reference, and field changes and additions can be made to the data. The massaged data can then be transmitted back to the computer.

74 Claims, 27 Drawing Figures



UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 4,016,542 Dated April 5, 1977

Inventor(s) Leo L. Azure, Jr.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the cover sheet in item [75] Inventor: "Leo L. Azure" should read -- Leo L. Azure, Jr. --.

Signed and Sealed this

Sixth Day of June 1978

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

DONALD W. BANNER
Commissioner of Patents and Trademarks

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,016,542
DATED : April 5, 1977
INVENTOR(S) : Leo L. Azure, Jr.

It is certified that error appears in the above—identified patent and that said Letters Patent is hereby corrected as shown below:

On The Title Page, Item 73, should read

-- Assignee: Azurdata, Incorporated --.

Signed and Sealed this

Twenty-ninth Day of *April 1980*

[SEAL]

Attest:

SIDNEY A. DIAMOND

Attesting Officer *Commissioner of Patents and Trademarks*

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 4,016,542 Dated April 5, 1977

Inventor(s) Leo L. Azure, Jr.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the "Abstract", line 22, change "input-out-" to --input/out- --.

Column 1, line 16, change "procesing" to --processing--.

Column 2, line 15, change "wee" to --were--;

Column 2, line 30, change "case" to --cause--.

Column 3, line 32, change "seed" to --sed--.

Column 4, line 28, change "terface" to --terfaces--;

Column 4, line 28, change "ASCH" to --ASCII--.

Column 4, lines 66-67, change "keyboard entry portion of the portable data gathering device" to --control circuitry--.*

Column 6, line 26, change "automtically" to --automatically--.

Column 12, line 5, change "extend" to --extent--.

Column 14, line 41, change "mans" to --means--.

Column 18, line 51, change "nrmal" to --normal--;

Column 18, line 52, change "tippd" to --tipped--.

Column 19, line 22, change "(C_S)" to --$(\bar{C}_S)$--.

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 4,016,542 Dated April 5, 1977

Inventor(s) Leo L. Azure, Jr.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 20, line 11, change "$\overline{\text{XMIT*}}$" to -- $\overline{\text{XMIT*}}$ --.

Column 22, line 59, change "$\overline{\text{INCREm}}$" to -- $\overline{\text{INCREM}}$ --.

Signed and Sealed this

Twenty-seventh Day of *December 1977*

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

LUTRELLE F. PARKER
Acting Commissioner of Patents and Trademarks

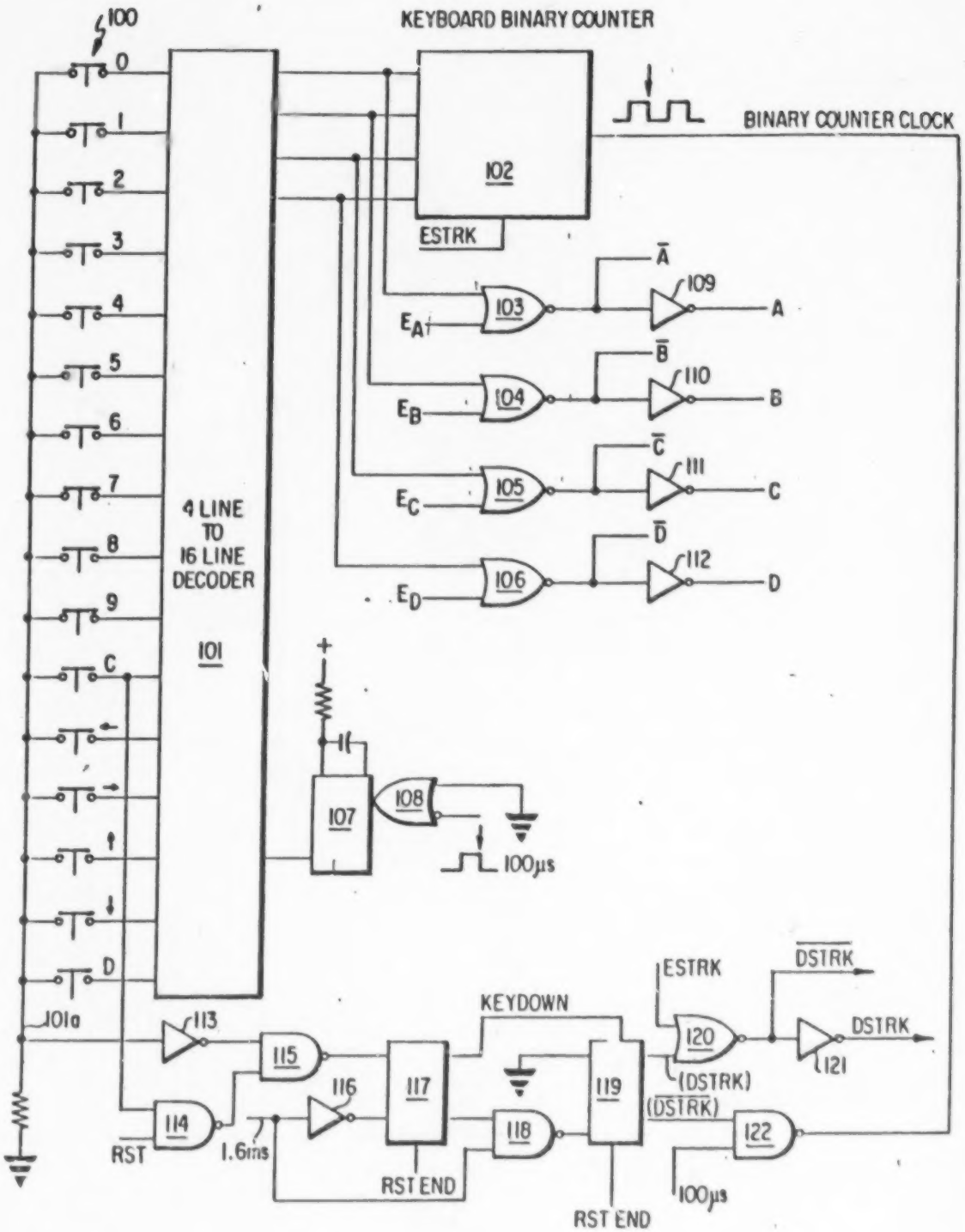

100
KEYBOARD BINARY COUNTER
BINARY COUNTER CLOCK
102
ESTRK
4 LINE TO 16 LINE DECODER
101
103
104
105
106
109
110
111
112
107
108
100μs
101a
113
114
115
116
117
118
119
120
121
122
RST
1.6ms
RST END
KEYDOWN
(DSTRK)
DSTRK
100μs

FIG.1A

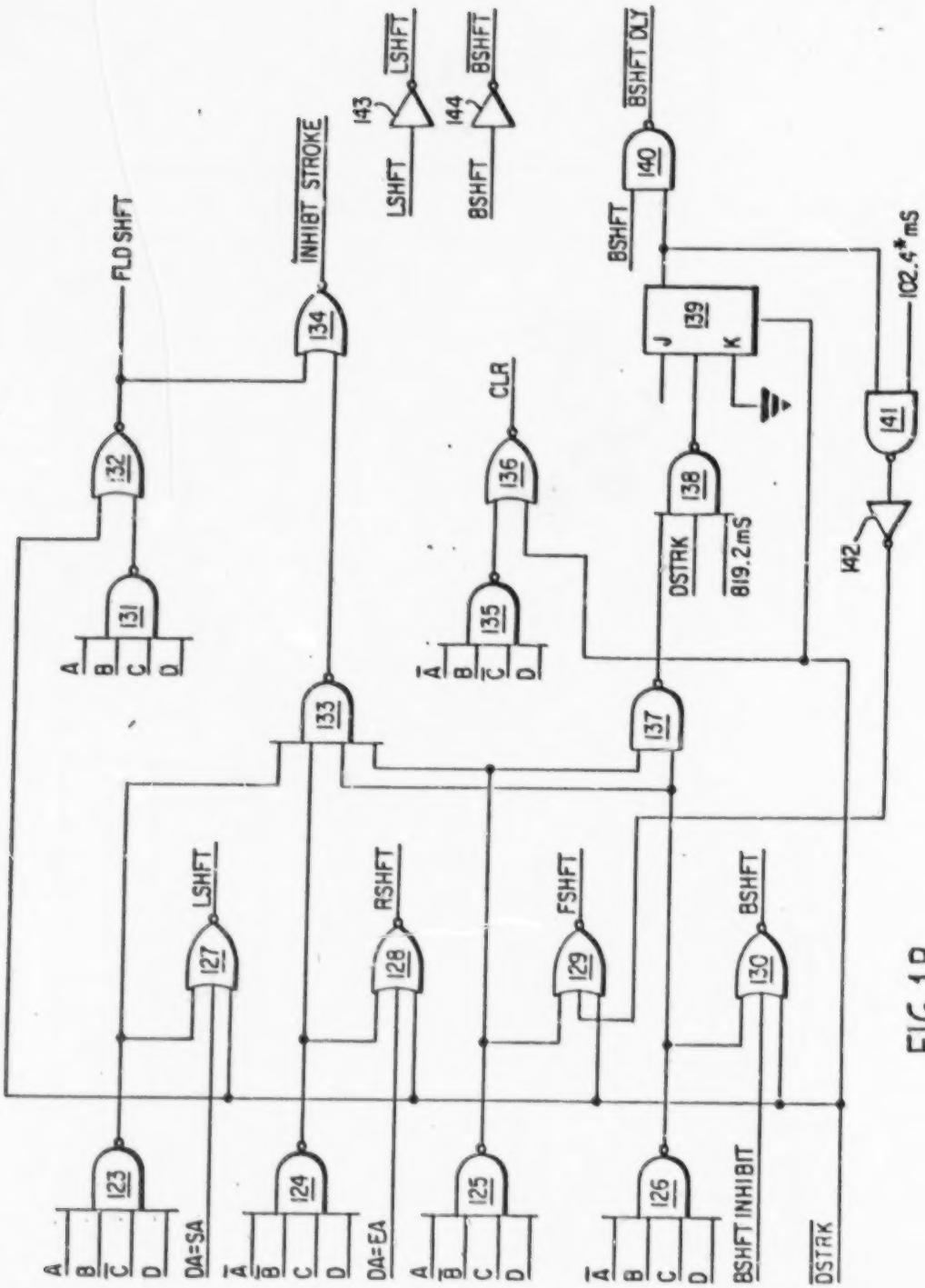

FLD SHFT
INHIBT STROKE
LSHFT
BSHFT
BSHFT DLY
CLR
DSTRK
819.2mS
102.4*mS
DA=SA
DA=EA
BSHFT INHIBIT
DSTRK
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144

FIG.1B

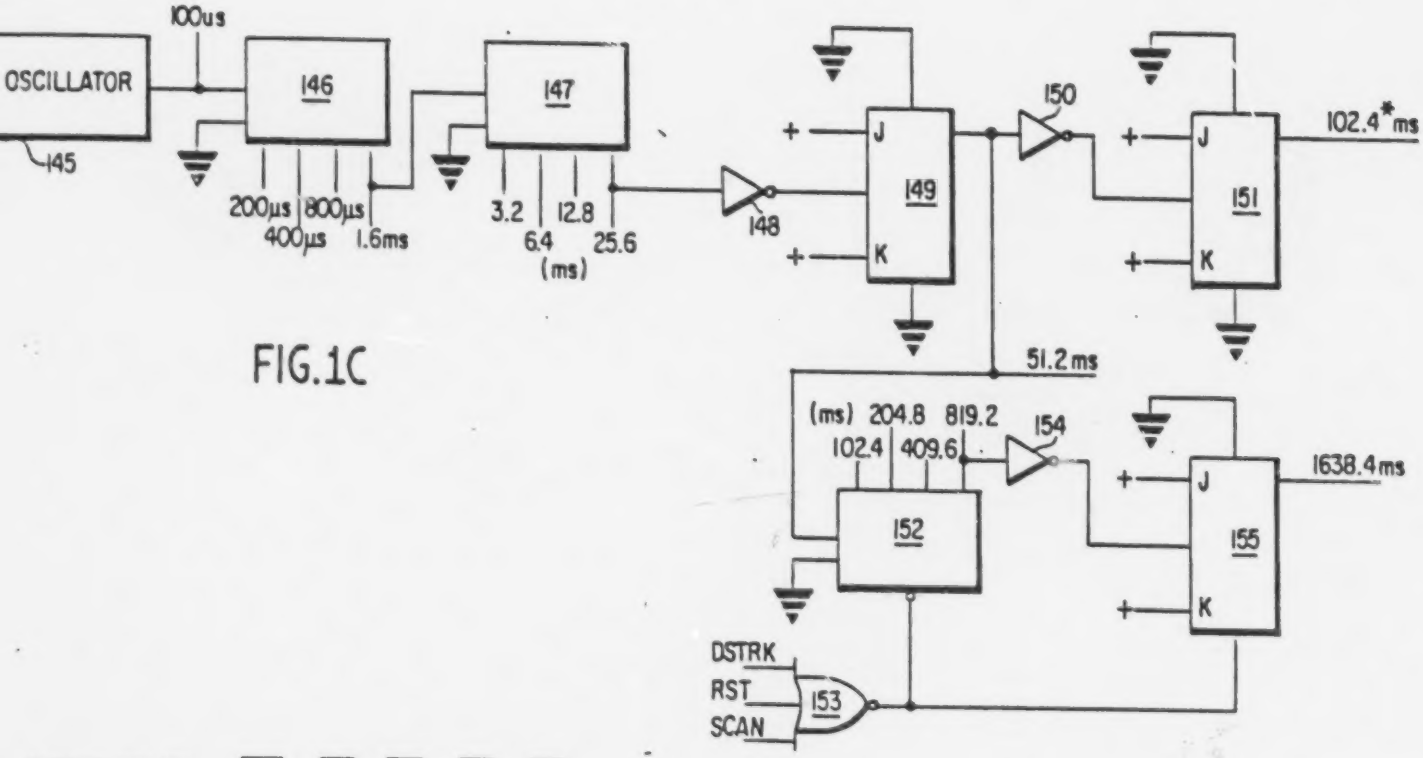

100us
OSCILLATOR
145
146
147
200µs
400µs
800µs
1.6ms
3.2
6.4
12.8
25.6
(ms)
148
149
150
151
102.4*ms
51.2ms
(ms) 204.8 819.2
102.4 409.6
154
152
155
1638.4ms
DSTRK
RST
SCAN
153
J
K

FIG.1C

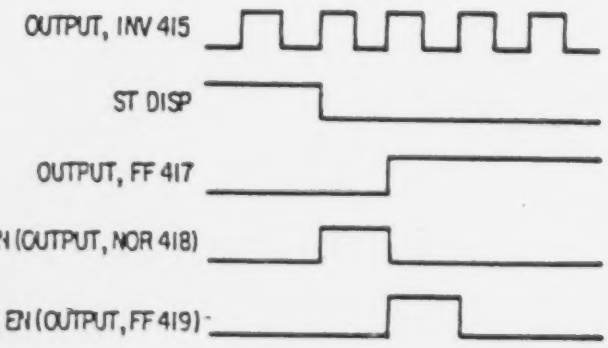

OUTPUT, INV 415
ST DISP
OUTPUT, FF 417
(OUTPUT, NOR 418)
EN (OUTPUT, FF 419)

FIG.3C

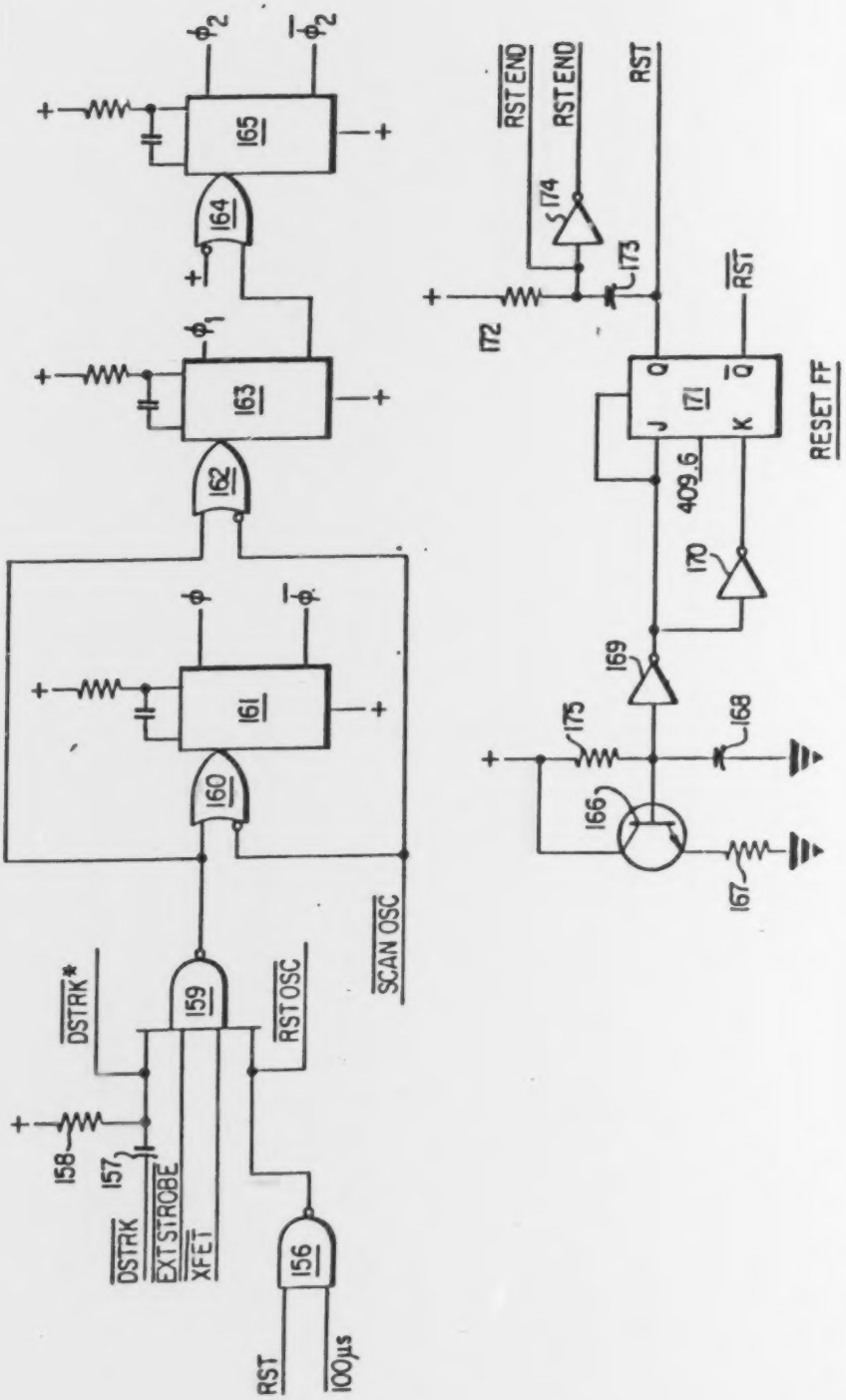

ϕ_2
$\overline{\phi_2}$
165
164
ϕ_1
163
162
ϕ
$\overline{\phi}$
161
160
159
156
158
157
DSTRK*
DSTRK
EXT STROBE
XFET
RST OSC
SCAN OSC
RST
100μs
RST END
RST END
RST
174
173
172
171
J
K
Q
$\overline{Q}$
RESET FF
$\overline{RST}$
409_6
170
169
175
168
166
167

FIG.1D

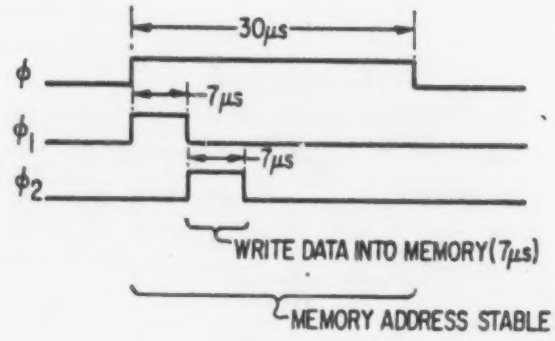

30μs
φ
7μs
φ1
7μs
φ2
WRITE DATA INTO MEMORY(7μs)
MEMORY ADDRESS STABLE (30μs)

FIG. 1E

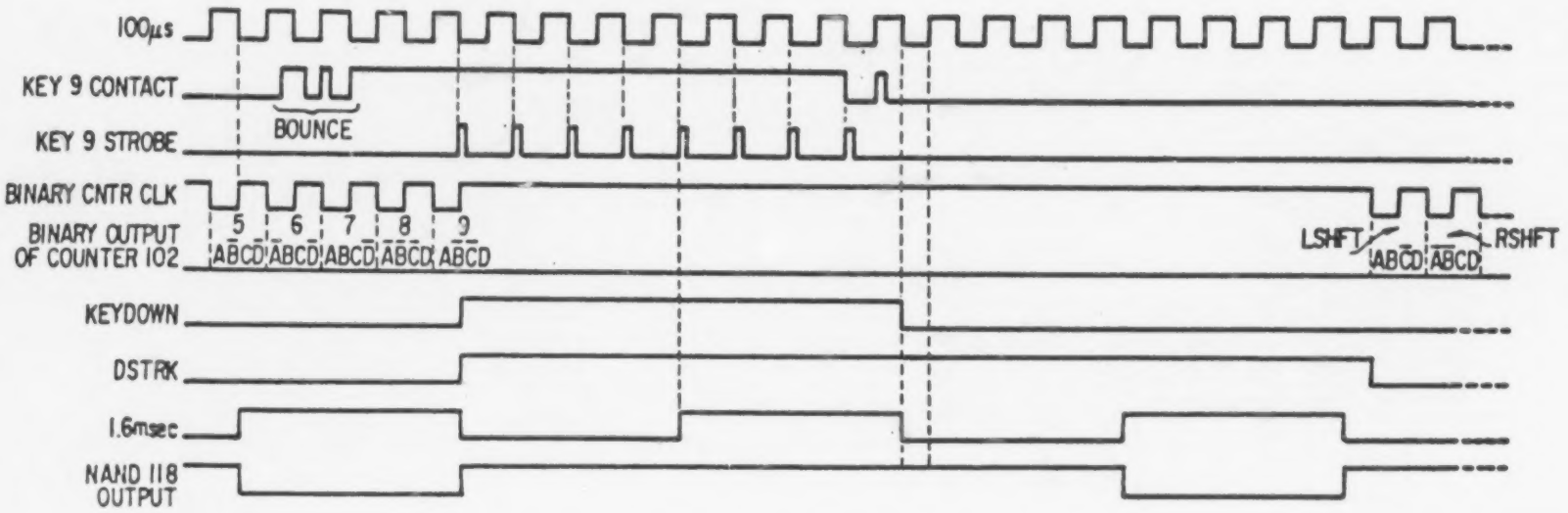

100μs
KEY 9 CONTACT
BOUNCE
KEY 9 STROBE
BINARY CNTR CLK
BINARY OUTPUT OF COUNTER 102
5 6 7 8 9
ABCD ABCD ABCD ABCD ABCD
LSHFT
RSHFT
ABCD ABCD
KEYDOWN
DSTRK
1.6msec
NAND 118 OUTPUT

FIG. 2A

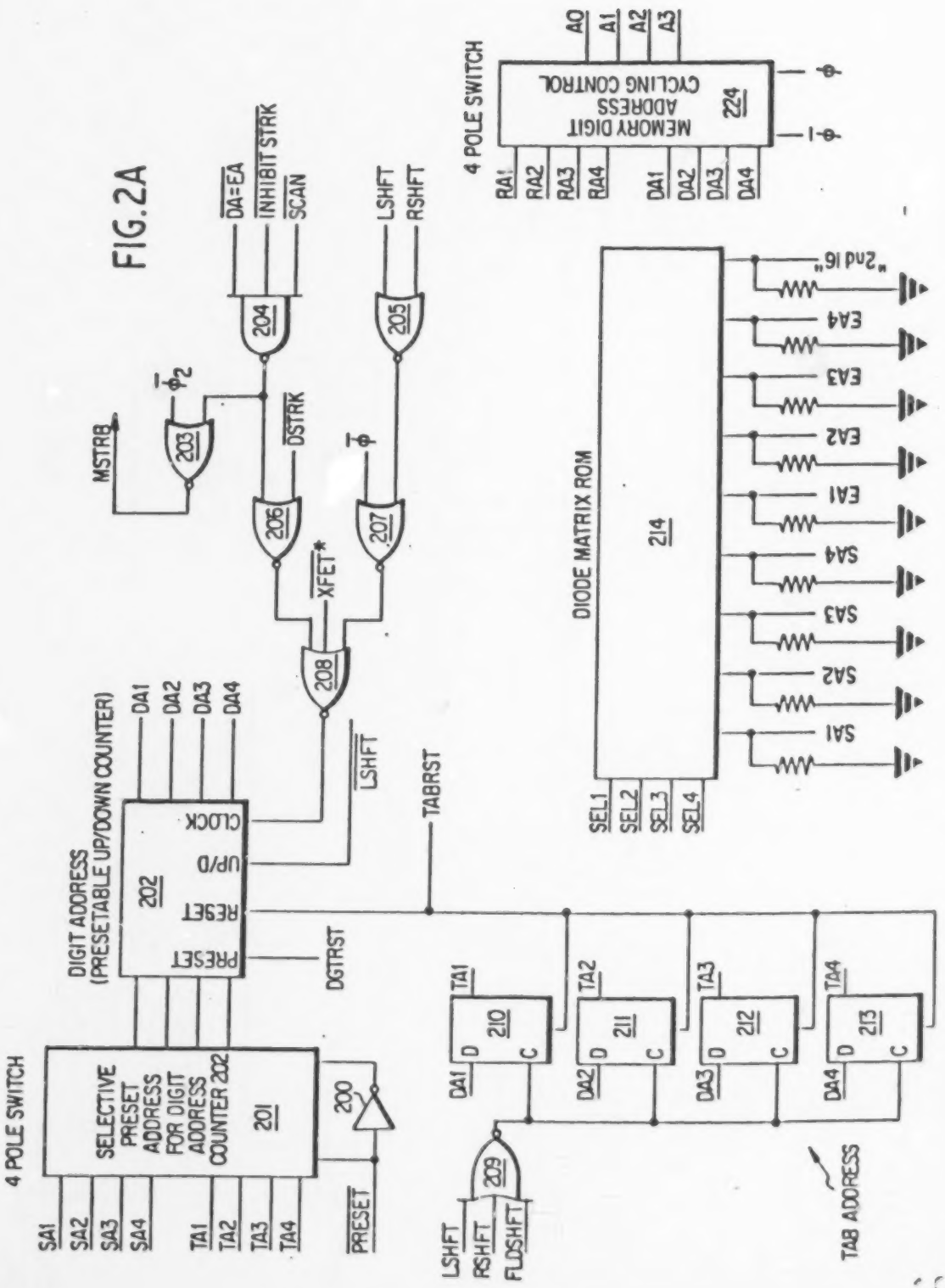
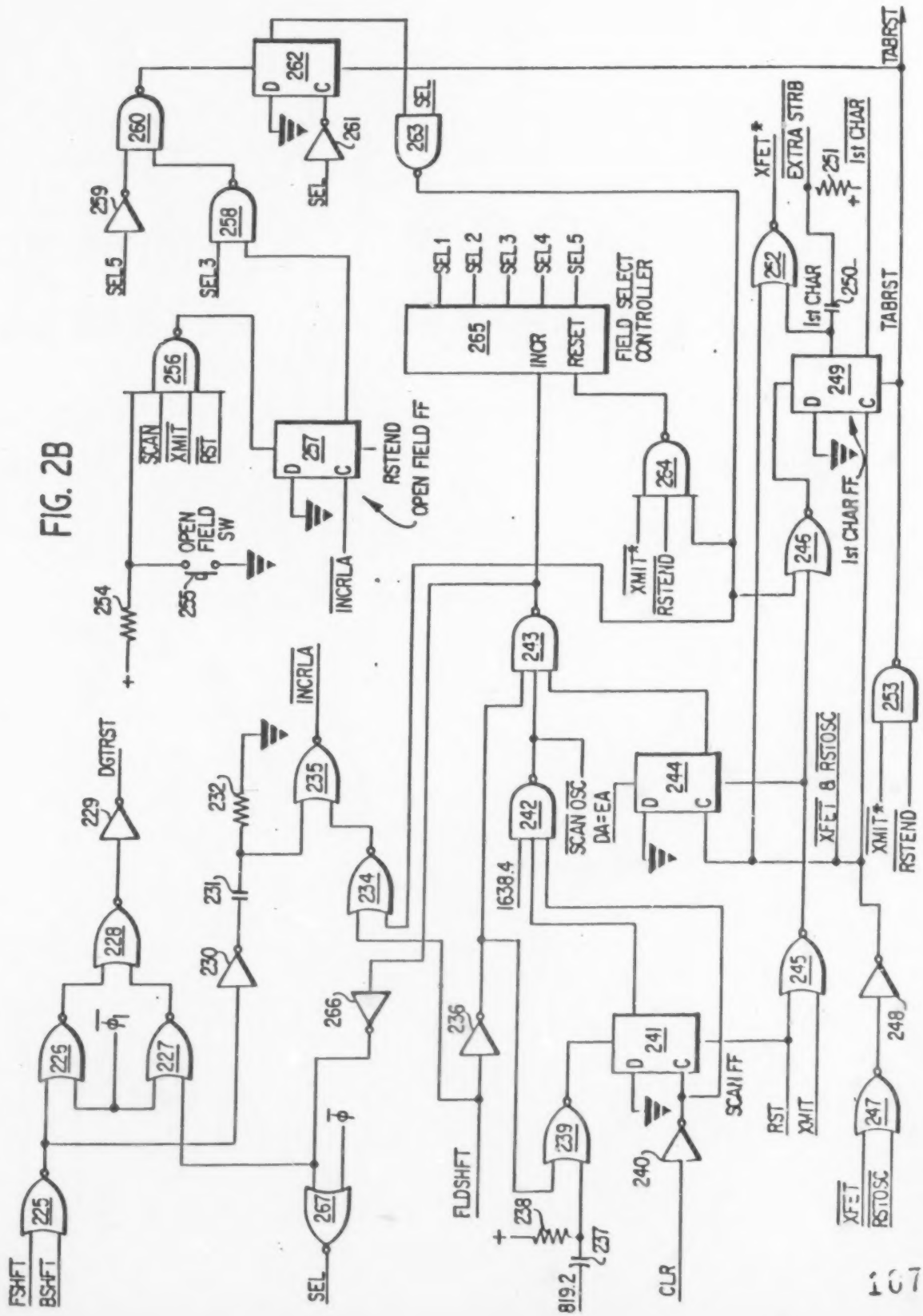

4 POLE SWITCH
SELECTIVE PRESET ADDRESS FOR DIGIT ADDRESS COUNTER 202
201
200
SA1
SA2
SA3
SA4
TA1
TA2
TA3
TA4
PRESET
DIGIT ADDRESS (PRESETABLE UP/DOWN COUNTER)
202
CLOCK
U/P/D
RESET
PRESET
DA1
DA2
DA3
DA4
DGTRST
TABRST
LSHFT
RSHFT
FLDSHFT
209
TA1
TA2
TA3
TA4
210
211
212
213
D
C
TAB ADDRESS
DIODE MATRIX ROM
214
SEL1
SEL2
SEL3
SEL4
"2nd 16"
EA4
EA3
EA2
EA1
SA4
SA3
SA2
SA1
4 POLE SWITCH
MEMORY DIGIT ADDRESS CYCLING CONTROL
224
A0
A1
A2
A3
RA1
RA2
RA3
RA4
DA1
DA2
DA3
DA4
φ
φ-1
MSTRB
203
$\overline{\phi_2}$
204
DA=EA
INHIBIT STRK
SCAN
DSTRK
205
LSHFT
RSHFT
206
207
$\overline{\phi}$
208
XFET*

FIG. 2B


FSHFT
BSHFT
225
226
227
228
229
DGTRST
230
231
232
234
235
INCRLA
254
255
OPEN FIELD SW
256
SCAN
XMIT
RST
257
RSTEND
OPEN FIELD FF
258
SEL3
259
SEL5
260
261
262
263
SEL
265
INCR
RESET
FIELD SELECT CONTROLLER
SEL1
SEL2
SEL3
SEL4
SEL5
264
XMIT*
RSTEND
243
242
1638.4
SCAN OSC
DA=EA
244
XFET & RSTOSC
236
266
267
FLDSHFT
238
819.2
237
239
240
241
SCAN FF
CLR
245
RST
XMIT
246
1st CHAR FF
247
XFET
RSTOSC
248
XMIT*
RSTEND
253
249
1st CHAR
250
TABRST
252
XFET*
EXTRA STRB
251
1st CHAR
TABRST

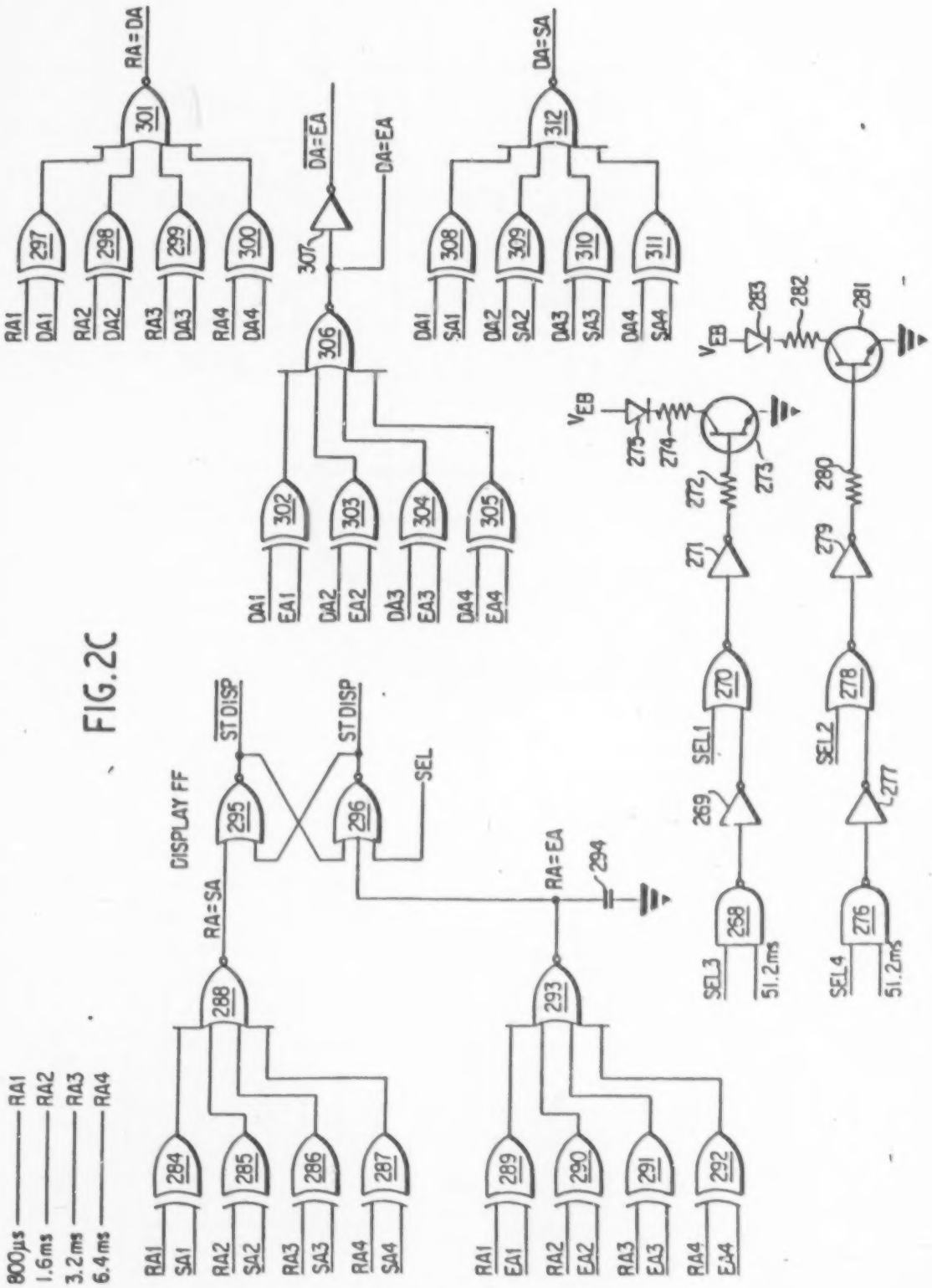

RA=DA
301
297
298
299
300
RA1
DA1
RA2
DA2
RA3
DA3
RA4
DA4
307
DA=EA
DA=EA
306
DA=SA
312
308
309
310
311
DA1
SA1
DA2
SA2
DA3
SA3
DA4
SA4
302
303
304
305
DA1
EA1
DA2
EA2
DA3
EA3
DA4
EA4
V_{EB}
283
282
281
275
274
273
272
280
271
279
270
278
SEL1
SEL2
269
277
SEL3
51.2ms
SEL4
51.2ms
298
276
ST DISP
ST DISP
SEL
DISPLAY FF
295
296
RA=SA
RA=EA
294
288
293
800μs
1.6ms
3.2ms
6.4ms
RA1
RA2
RA3
RA4
284
285
286
287
289
290
291
292
RA1
SA1
RA2
SA2
RA3
SA3
RA4
SA4
RA1
EA1
RA2
EA2
RA3
EA3
RA4
EA4

FIG. 2C

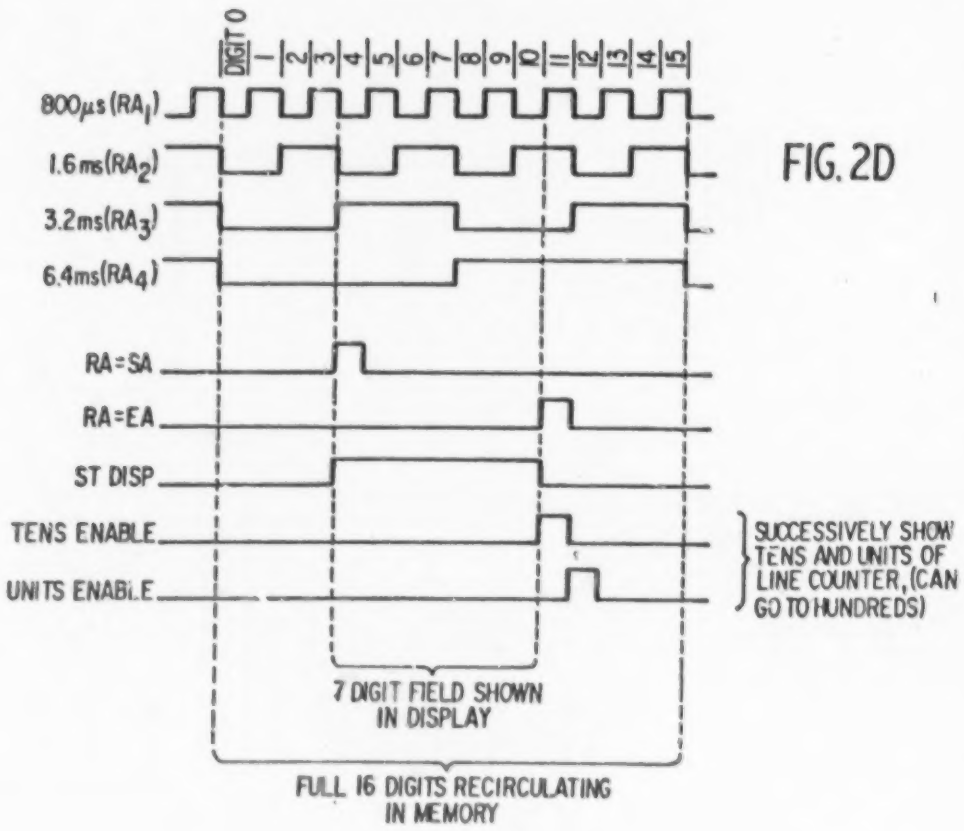
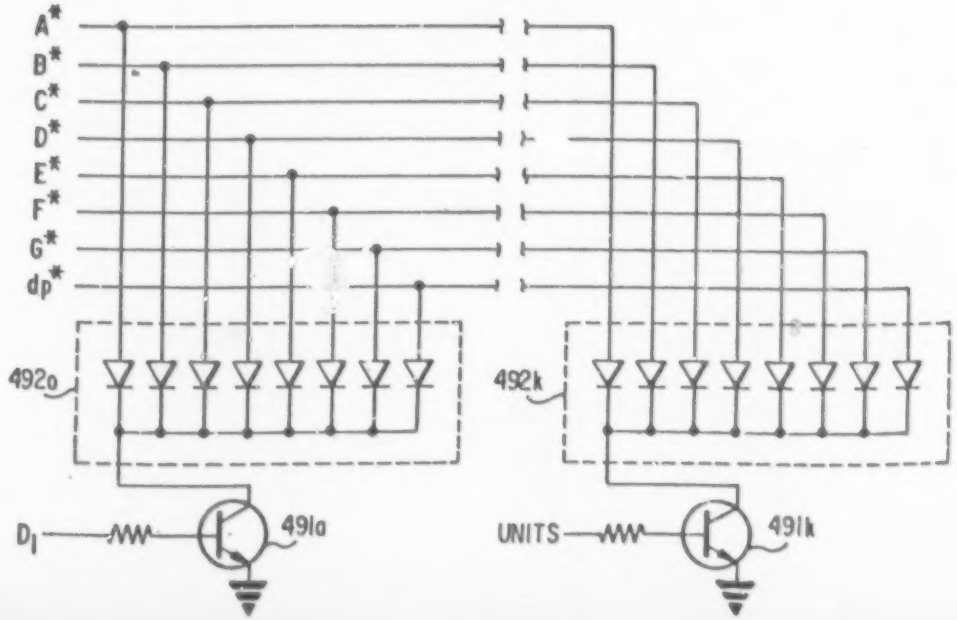

DIGIT 0
800μs (RA1)
1.6ms (RA2)
3.2ms (RA3)
6.4ms (RA4)
RA=SA
RA=EA
ST DISP
TENS ENABLE
UNITS ENABLE
SUCCESSIVELY SHOW TENS AND UNITS OF LINE COUNTER, (CAN GO TO HUNDREDS)
7 DIGIT FIELD SHOWN IN DISPLAY
FULL 16 DIGITS RECIRCULATING IN MEMORY

FIG. 2D

FIG. 3D


A*
B*
C*
D*
E*
F*
G*
dp*
492o
492k
D1
491o
UNITS
491k

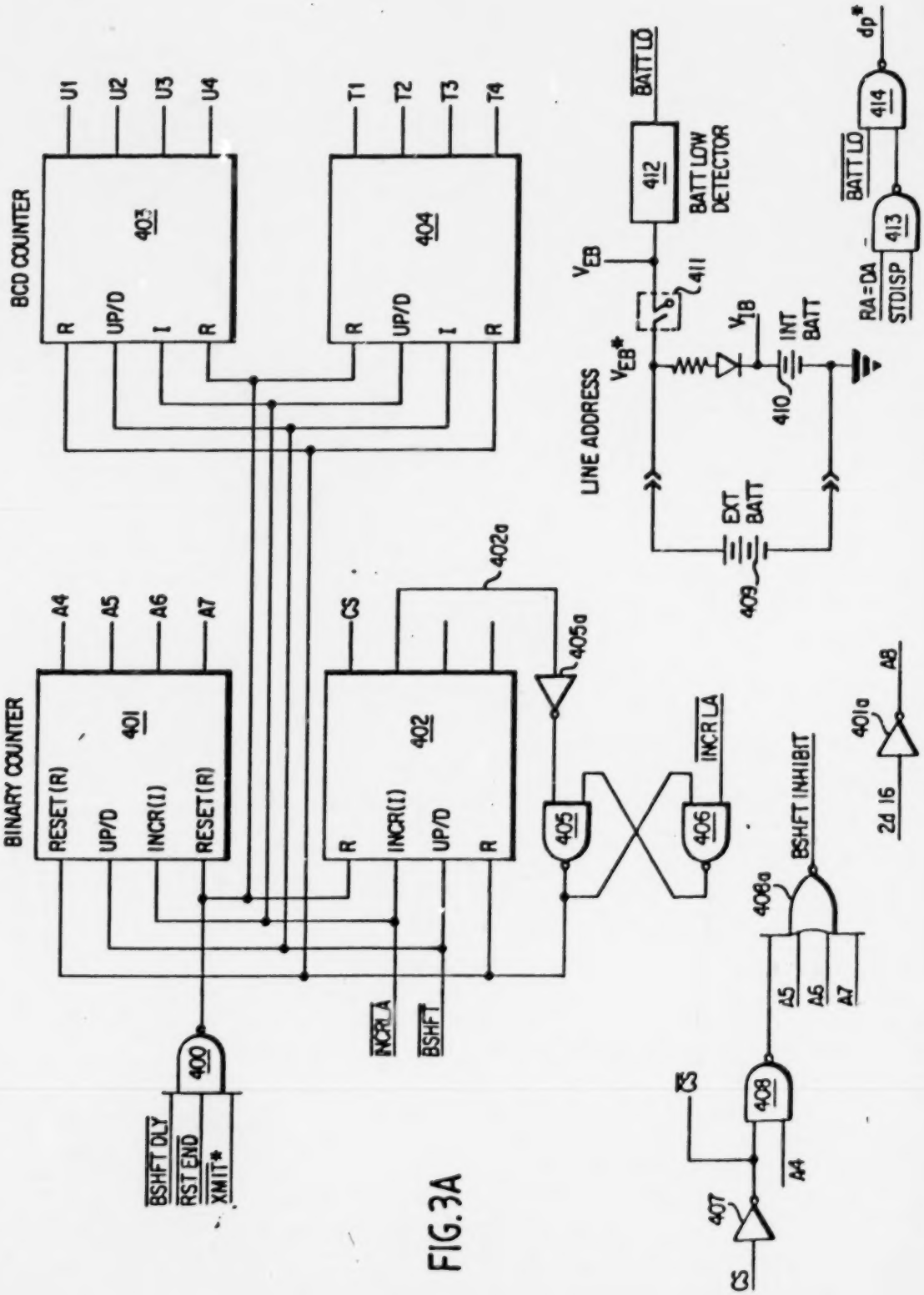

BCD COUNTER
403
404
U1
U2
U3
U4
T1
T2
T3
T4
R
UP/D
I
BINARY COUNTER
401
402
A4
A5
A6
A7
CS
RESET(R)
INCR(I)
402a
405a
405
406
INCR LA
BSHFT
400
BSHFT DLY
RST END
XMIT*
BATT LO
412
BATT LOW DETECTOR
VEB
411
VEB*
VIB
INT BATT
410
LINE ADDRESS
EXT BATT
409
414
dp*
413
RA=DA
STDISP
401a
A8
24 16
BSHFT INHIBIT
408a
408
407
A4
A5
A6
A7

FIG. 3A

110

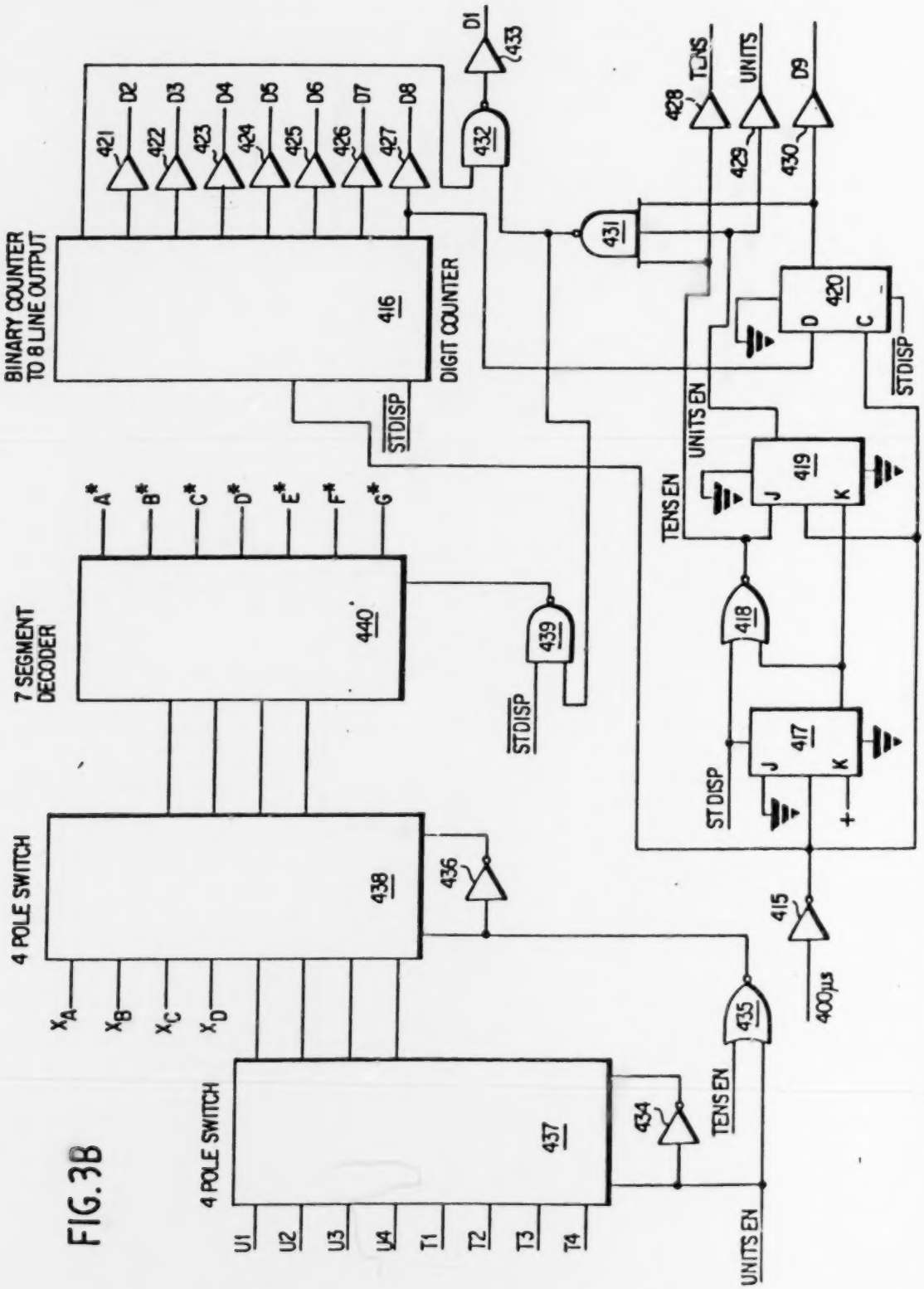

BINARY COUNTER TO 8 LINE OUTPUT
416
DIGIT COUNTER
STDISP
D1
D2
D3
D4
D5
D6
D7
D8
421
422
423
424
425
426
427
428
429
430
431
432
433
TENS
UNITS
D9
420
D
C
STDISP
UNITS EN
TENS EN
419
J
K
418
417
ST DISP
+
415
400µs
7 SEGMENT DECODER
440
A*
B*
C*
D*
E*
F*
G*
439
STDISP
4 POLE SWITCH
438
436
X_A
X_B
X_C
X_D
435
TENS EN
4 POLE SWITCH
437
434
U1
U2
U3
U4
T1
T2
T3
T4
UNITS EN

FIG. 3B

FIG.4A

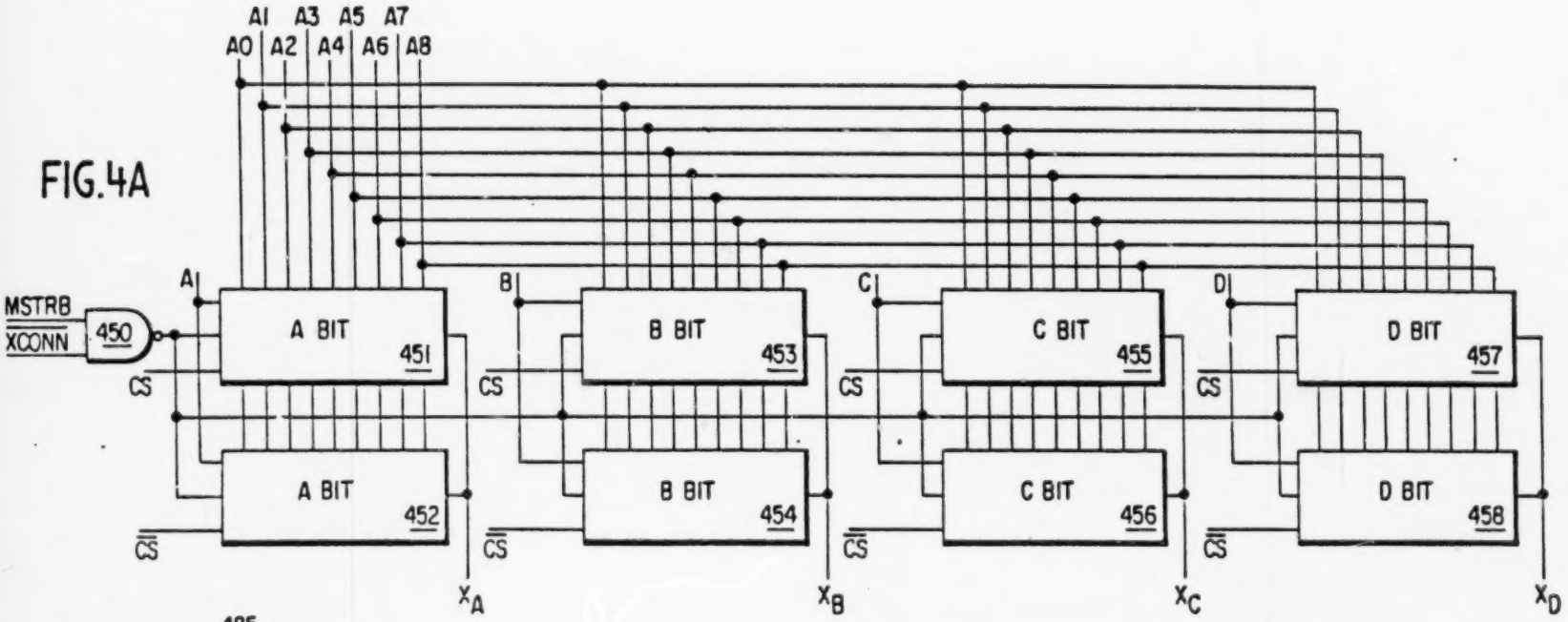
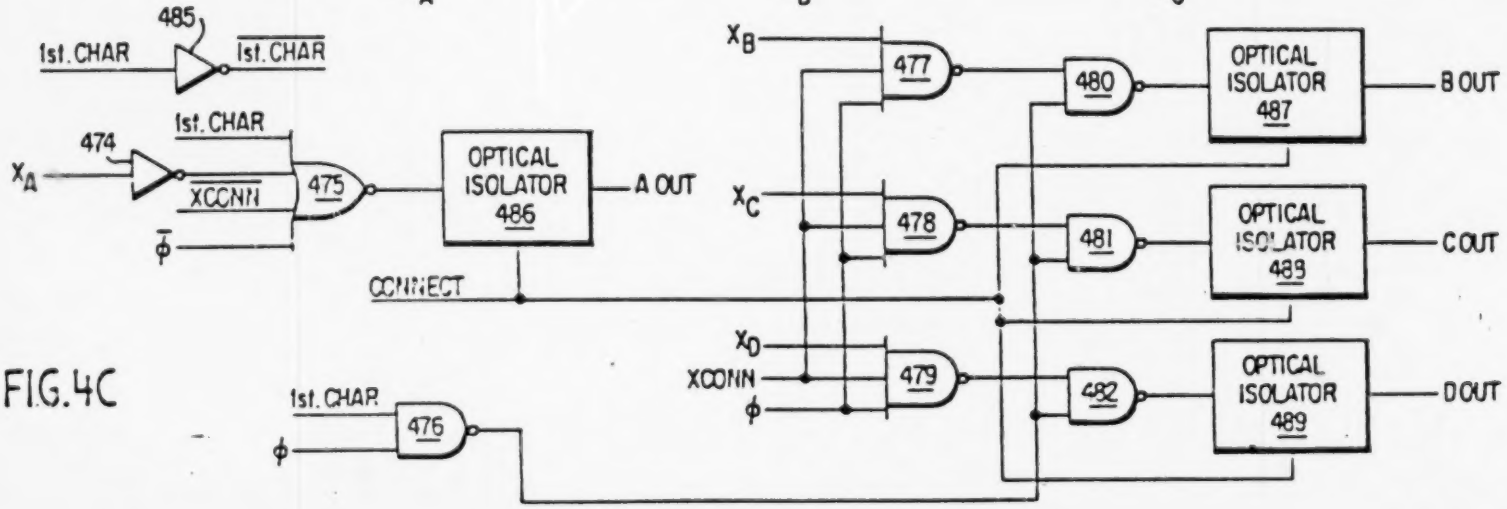


FIG.4C



112

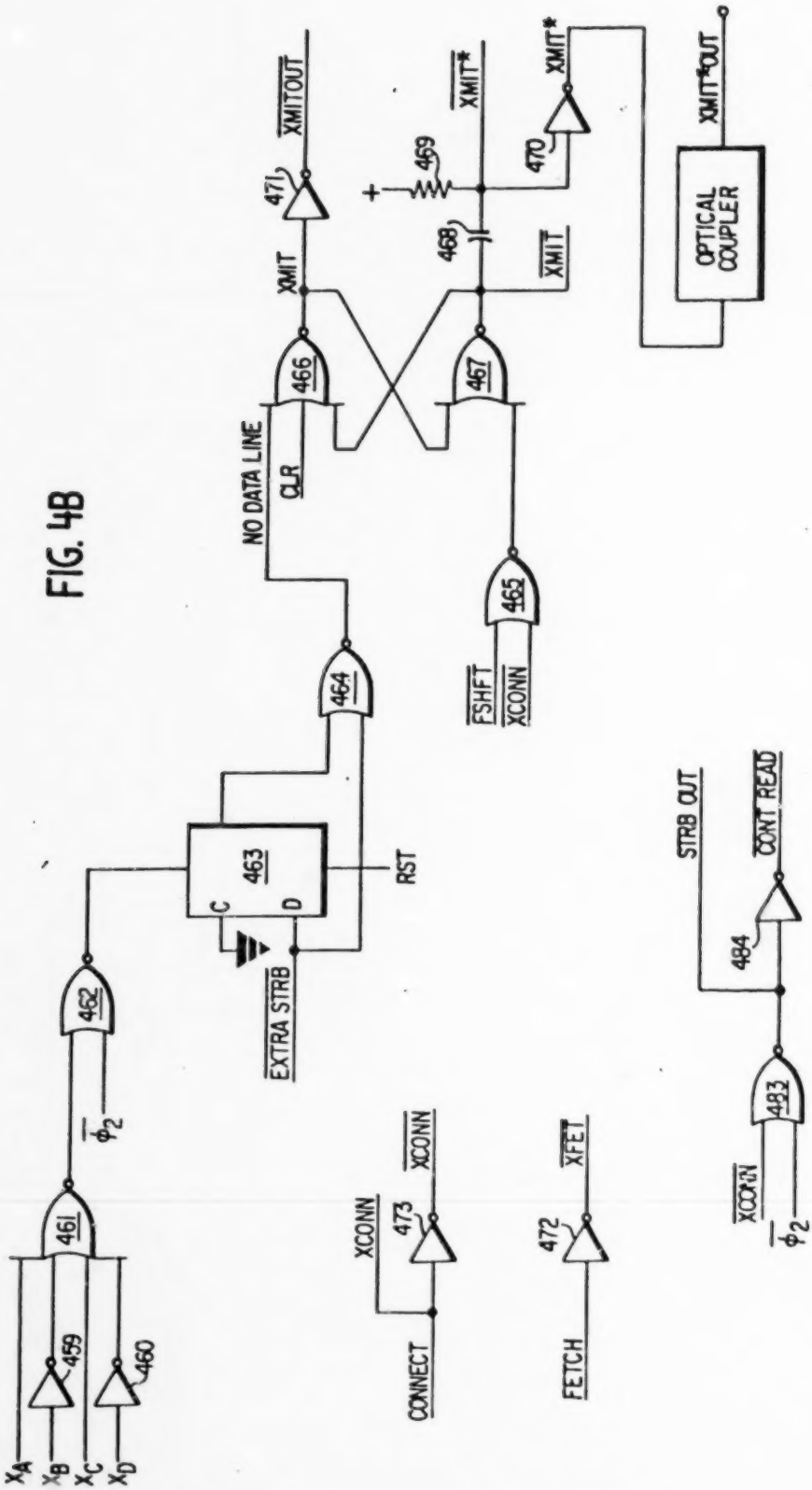

XA
XB
XC
XD
459
460
461
462
φ2
463
C
D
RST
EXTRA STRB
464
NO DATA LINE
CLR
466
XMIT
471
XMITOUT
468
469
XMIT*
470
XMIT*
XMIT
467
465
FSHIFT
XCONN
OPTICAL COUPLER
XMIT*OUT
XCONN
473
XCONN
CONNECT
472
XFET
FETCH
STRB OUT
CONT READ
484
483
XCONN
φ2

FIG. 4B

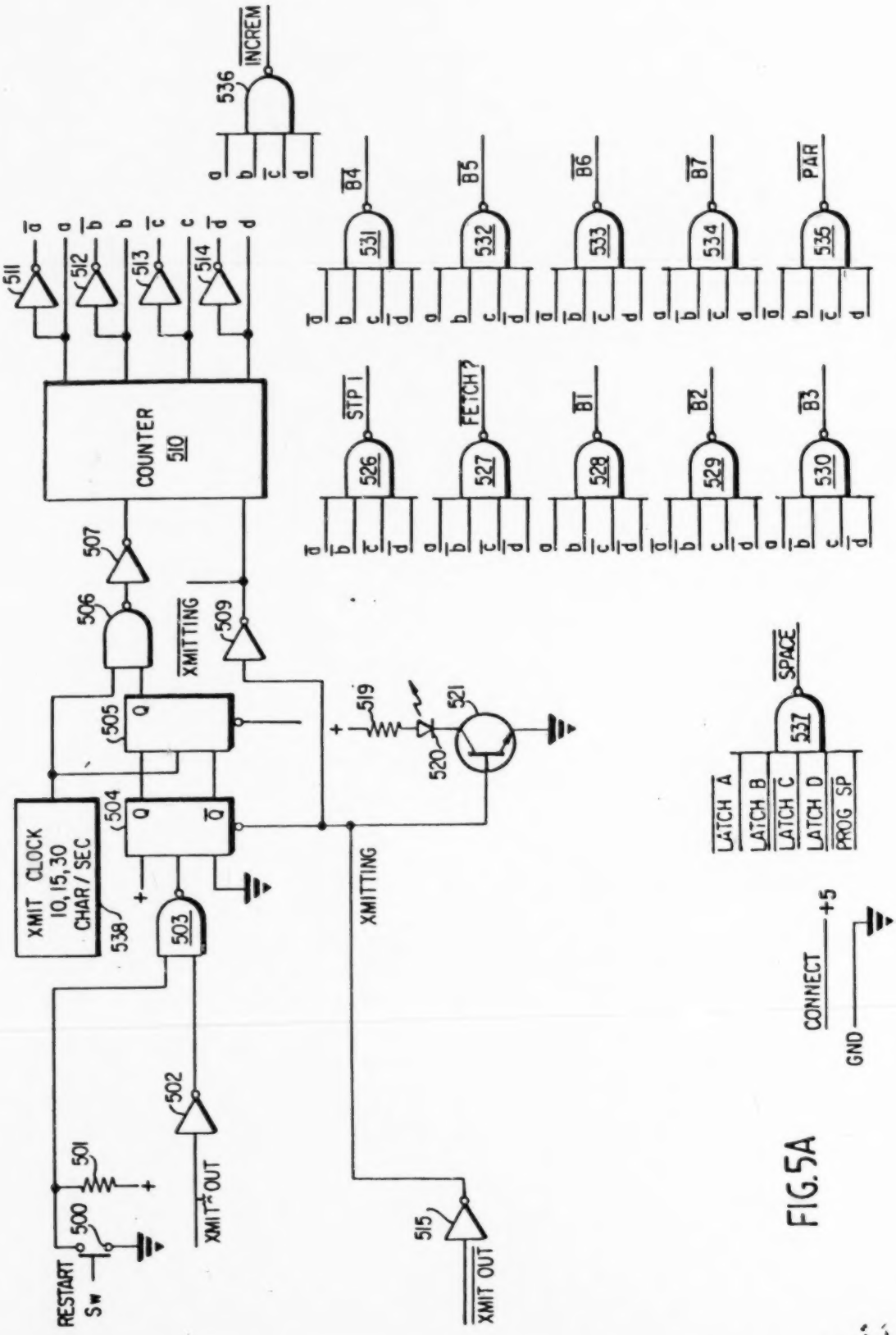

RESTART SW
500
501
+
502
XMIT* OUT
503
XMIT CLOCK 10, 15, 30 CHAR/SEC
538
504
505
506
507
COUNTER 510
511
512
513
514
XMITTING
509
519
520
521
XMITTING
515
XMIT OUT
536 INCREM
531 B4
532 B5
533 B6
534 B7
535 PAR
526 STP I
527 FETCH?
528 B1
529 B2
530 B3
LATCH A
LATCH B
LATCH C
LATCH D
PROG SP
537 SPACE
CONNECT +5
GND

FIG. 5A

CLEAR
CH CNTR
570
571
XMITTING
569
L/F*
565
568
L/F*
CLK IN
564
567
566
573
DETECT L
DETECT L
574
LN CNTR
575
XMITTING
558
559
560
561
562
563
INCREM
L/F LINE
RO1
RO2
C/R
RO2
RO1
L/F
C/R
557
556
555
554
553
XMITTING
FETCH END
543
LATCH A
LATCH B
LATCH C
LATCH D
LATCH A
LATCH B
LATCH C
542
540
539
541
B CONT
C CONT
D CONT
A CONT
CONT READ2
A OUT
B OUT
C OUT
D OUT
FETCH
548
546
545
FETCH
544
547
FETCH?
FETCH
552
551
550
549
A CONT
B CONT
C CONT
D CONT
PROG LF
RESTART
PROG SP
C/R
L/F
RO1
RO2

FIG. 5B

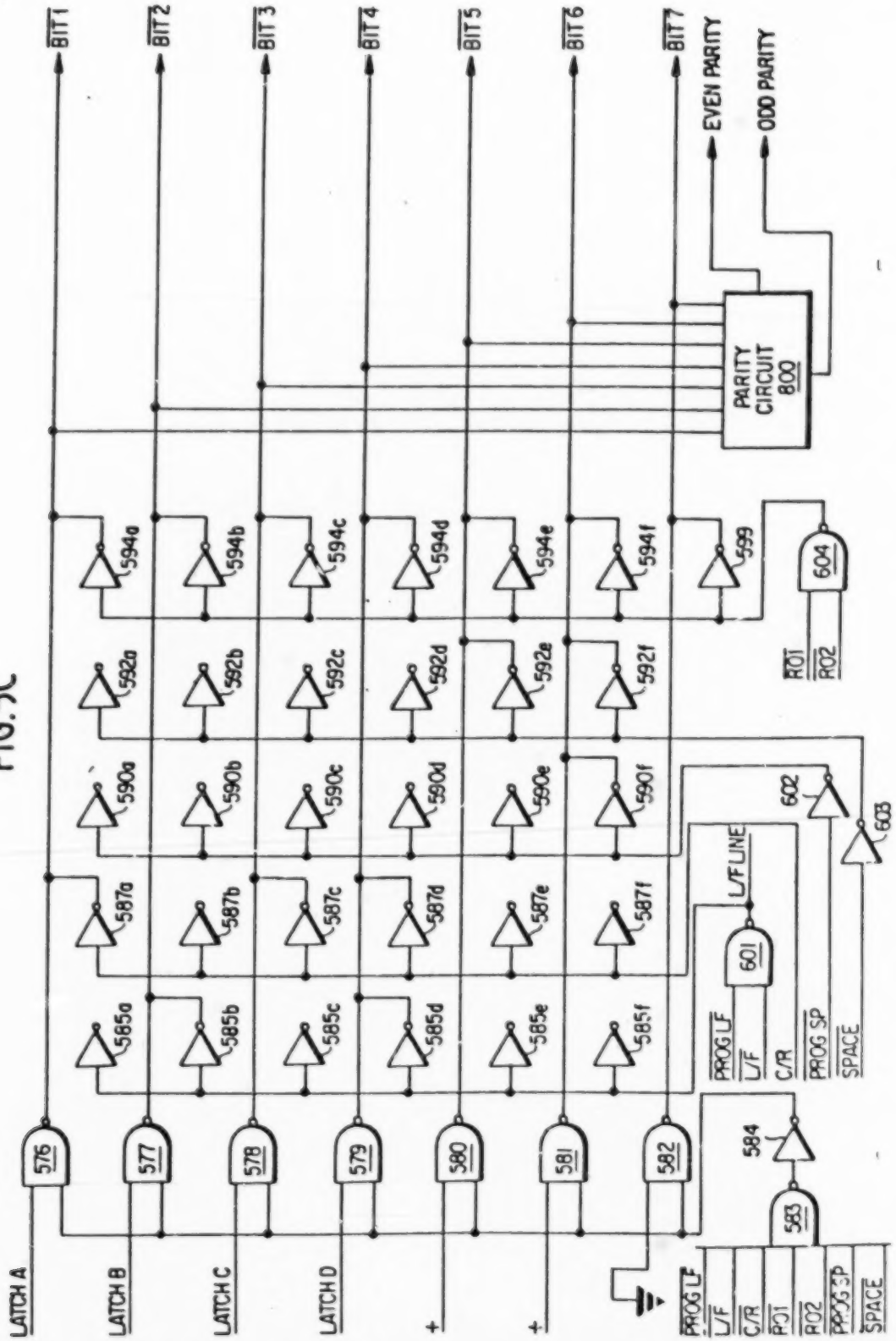

BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
EVEN PARITY
ODD PARITY
PARITY CIRCUIT 800
LATCH A
LATCH B
LATCH C
LATCH D
576
577
578
579
580
581
582
583
584
585a
585b
585c
585d
585e
585f
587a
587b
587c
587d
587e
587f
590a
590b
590c
590d
590e
590f
592a
592b
592c
592d
592e
592f
594a
594b
594c
594d
594e
594f
599
601
602
603
604
L/F LINE
PROG L/F
L/F
C/R
PROG SP
SPACE
R01
R02

FIG. 5C

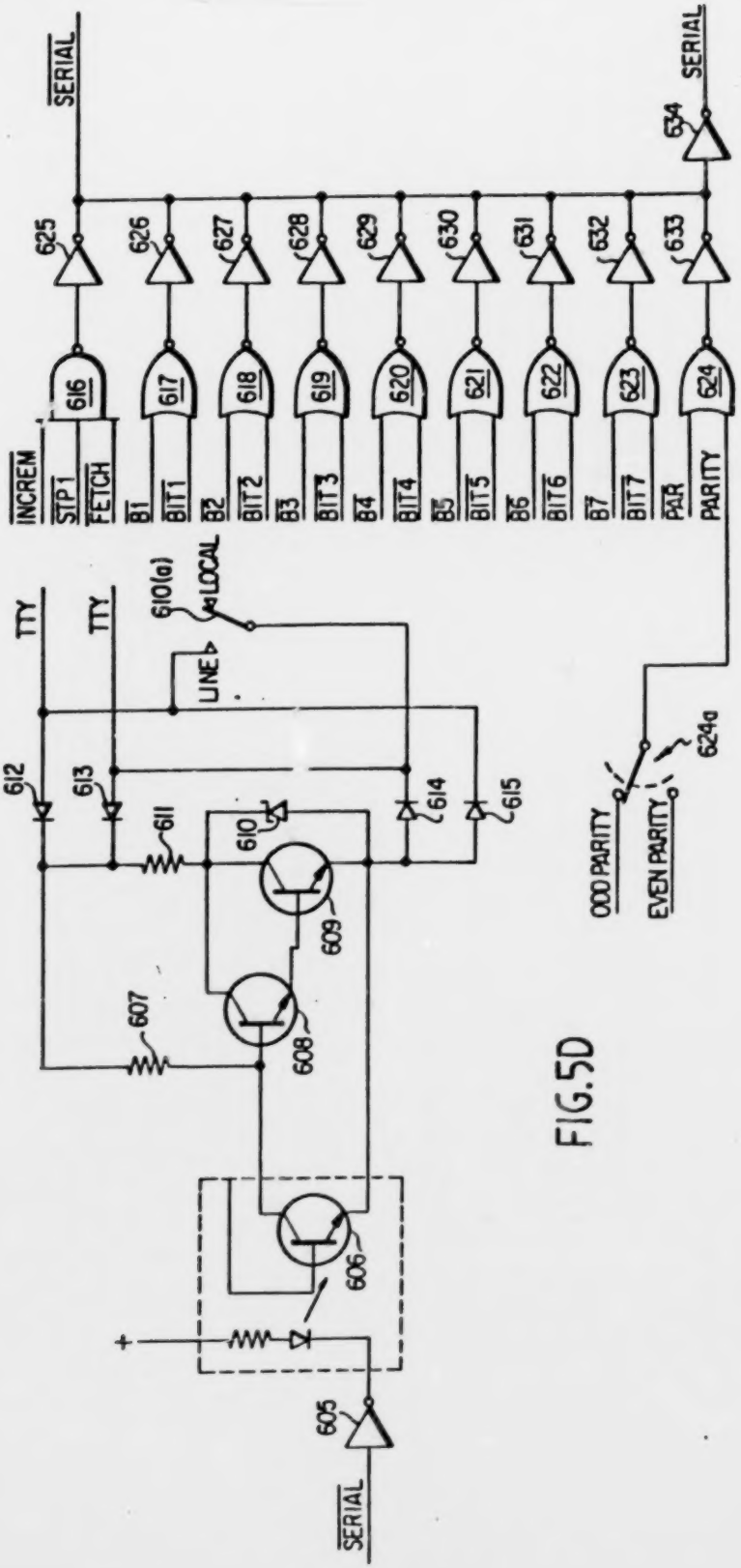

SERIAL
625
626
627
628
629
630
631
632
633
634
SERIAL
INCREM
STP1
FETCH
616
617
618
619
620
621
622
623
624
B1
BIT1
B2
BIT2
B3
BIT3
B4
BIT4
B5
BIT5
B6
BIT6
B7
BIT7
PAR
PARITY
TTY
TTY
610(a)
LOCAL
LINE
612
613
611
610
614
615
609
607
608
606
605
SERIAL
624a
ODD PARITY
EVEN PARITY

FIG. 5D

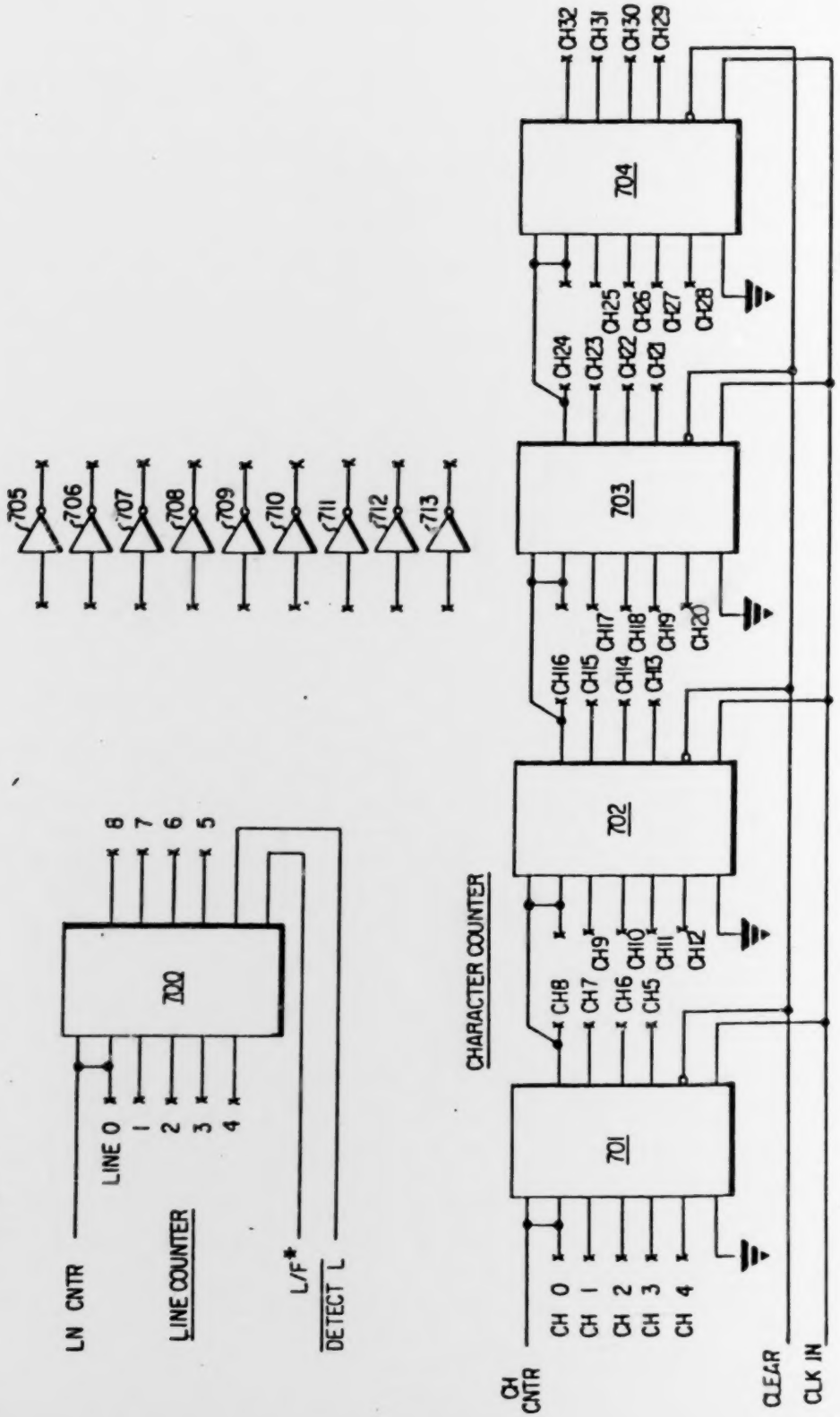

CH32
CH31
CH30
CH29
704
CH25
CH26
CH27
CH28
CH24
CH23
CH22
CH21
703
705
706
707
708
709
710
711
712
713
CH16
CH15
CH14
CH13
CH17
CH18
CH19
CH20
702
CHARACTER COUNTER
CH8
CH7
CH6
CH5
CH9
CH10
CH11
CH12
701
CH 0
CH 1
CH 2
CH 3
CH 4
CH CNTR
CLEAR
CLK IN
LN CNTR
LINE 0
1
2
3
4
LINE COUNTER
700
8
7
6
5
L/F*
DETECT L

FIG. 5E

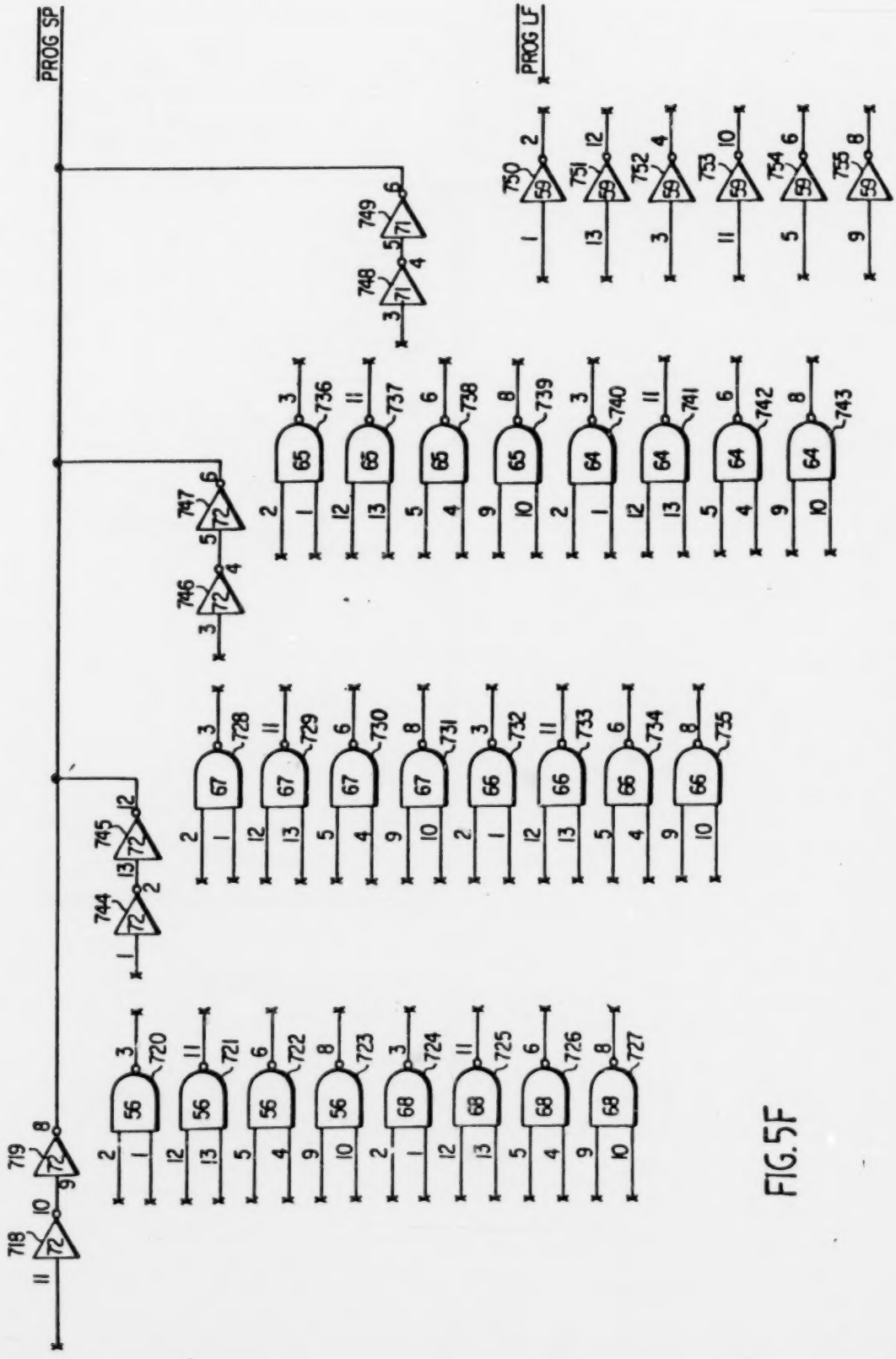


FIG. 5F

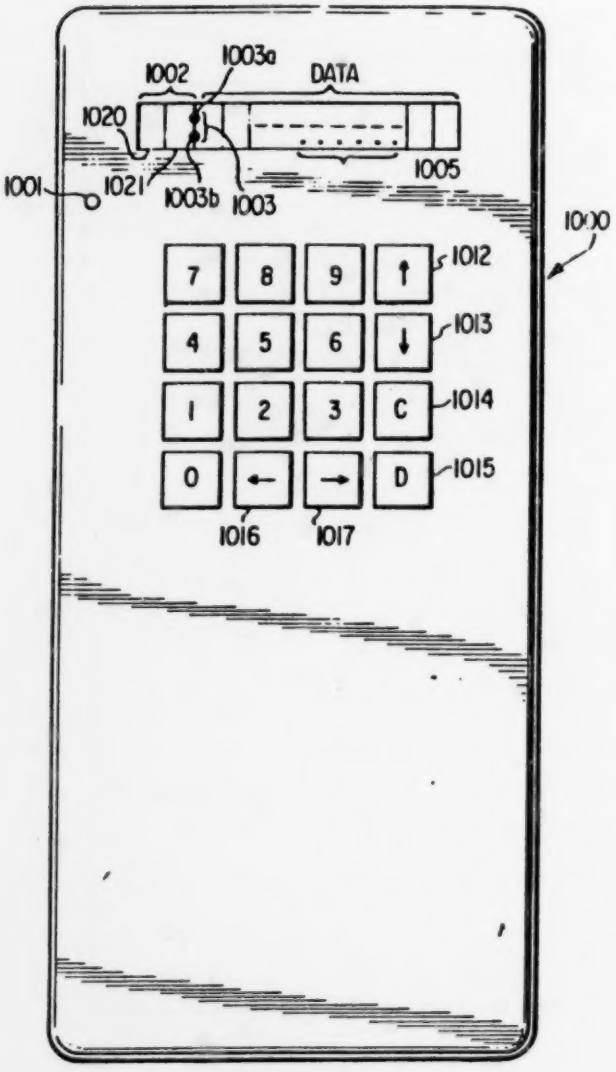
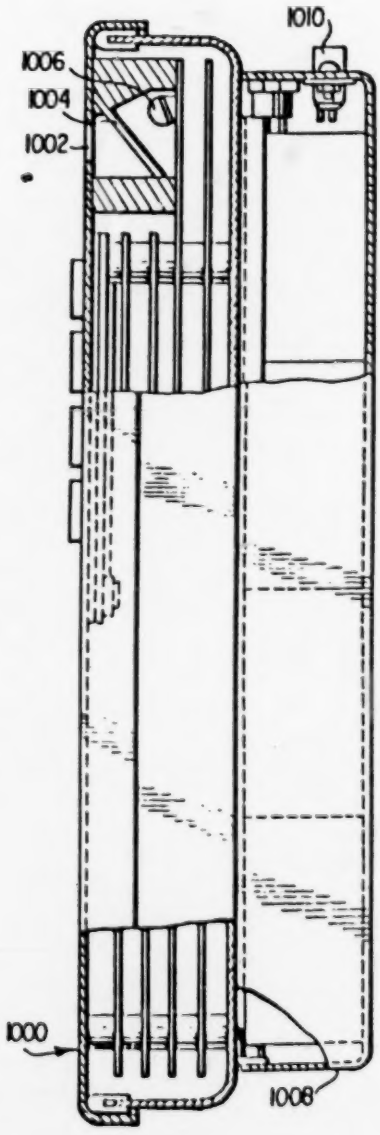

1003a
1002
DATA
1020
1005
1001
1021
1003b
1003
1000
7
8
9
1012
4
5
6
1013
1
2
3
C
1014
0
D
1015
1016
1017

FIG. 6A

FIG. 6B


1010
1006
1004
1002
1000
1008

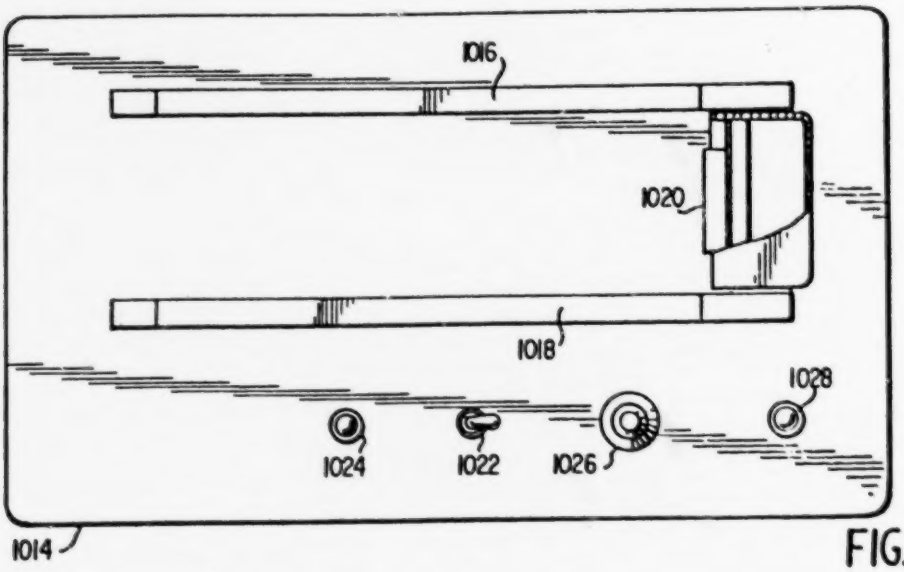


FIG. 7A

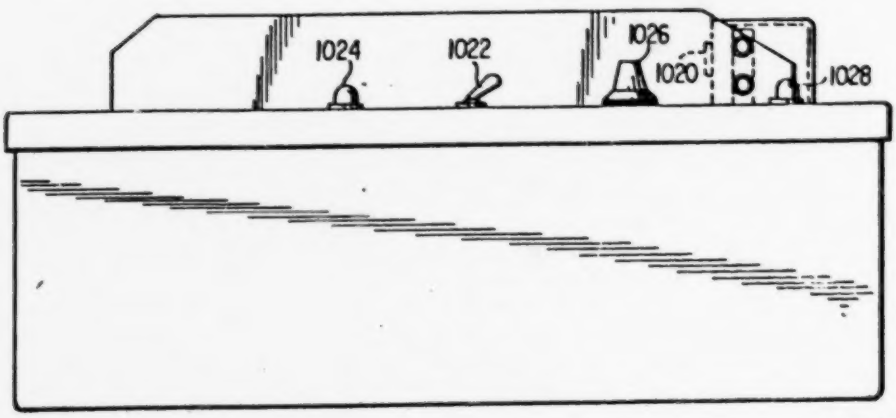
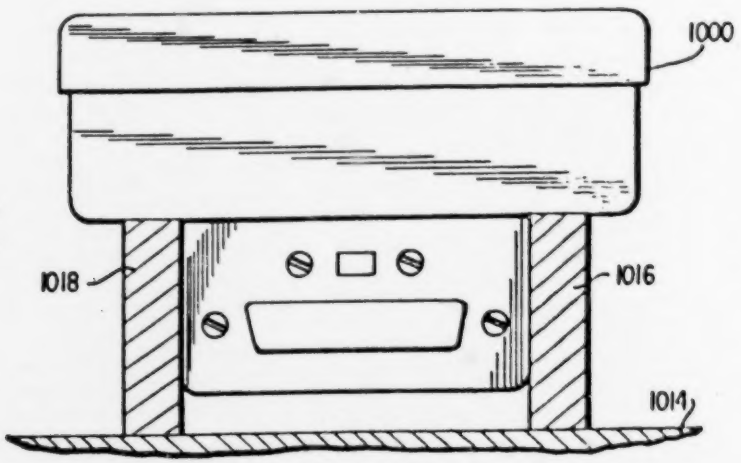


FIG. 7B

FIG. 7C



ELECTRONIC NOTEBOOK FOR USE IN DATA GATHERING, FORMATTING AND TRANSMITTING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a data storage and transmission system and, more particularly, to such a system including a hand-held portable device operable as an electronic notebook, for storing a large amount of data, entered manually by keyboard or automatically by transmission through an input/output connector, and which may be read out automatically at a remote terminal for immediate transmission of the data to a distant central processing system, and/or for storing and/or preparing a hard copy data print-out at the remote terminal

2. State of the Prior Art

In the prior art, the collection or gathering of data, particularly from remote locations for subsequent transmission to a central processing system, presents the problem that the gathered data, at some point in the operation, must be manually translated into computer compatible form. Typically, the data first is recorded manually on special forms which then are taken to a central facility where the data contained thereon must be converted into computer compatible form, usually by keypunching the data onto computer cards. Manual conversion is extremely costly, is a major source of error, and delays the availability of the data for subsequent processing

Raw material inventory control, as in the forest products industry, requires that each log be measured and recorded, along with several descriptors. The speed of processing the raw materials in this and other industries often exceeds that of processing the collected data, with the result that the raw material is turned ino finished products before the inventory reports are completed. Other applications include re-ordering of goods in grocery stores; monitor station reading for pollution control; meter reading in gas and electric utilities; route sales orders, such as for perishable goods distributors; trouble reporting, such as in police work, highway construction and repair, and telephone and power industries, and data collection in scientific research.

In a typical meter reading application it is required that the meter reader carry information fixed data with him related to each stop on his route for that day, including the house number, meter number, previous meter reading, a code for the location of the meter, and warning codes such as for a mad dog. This information can be loaded into the first field of each line of the memory of the electonic notebook from a computer, prior to proceeding on the route. The corresponding line then is displayed in use at each route stop, and the meter reading (variable data) would be entered into a second field. At the end of the collection period, the fixed data and variable data for each meter would be transmitted to the computer.

Portable key-to-magnetic tape devices have gained acceptance in certain areas, such as the grocery retail industry for use in re-ordering inventory, replacing the order forms, mails, and keypunching where the operating environment permits the use of magnetic tape recorders. However, in most applications magnetic tape recording imposes too many constraints. Temperature, shock, water and dust all cause problems to tape recorders. But more importantly, key-to-tape machines do not have the versatility or ease of use to make them widely accepted as electronic notebooks. The size and weight of the tape recorder requires that shoulder straps and slings be used to carry the recorder, and an umbilical cord attaches the recorder to the hand-held keyboard. Further, data recall and random access to data in memory, a "must" for a true electonic notebook, are not possible with magnetic tape memories. A true electronic notebook, such as the present data collection device, must emulate a note pad in versatility, size and weight, else the manmachine interface problem will limit acceptance — as key-to-tape machines have been limited to grocery stores

Most of the available key-to-tape units were designed several years ago before many advances in solid state memory technology had occurred. During 1973, some limited feature solid state units have appeared on the market, designed for the grocery store application. They have not be designed as electronic notebooks, but as solid state equivalents to the old magnetic tape units.

Another prior art source data entry means is the optical reader, which reads source data, marked or written on a document directly into a computer. Keypunch and other secondary operation costs asociated with entering data are eliminated. However, optical reading is viable only where certain constraints can be tolerated. For example, the environmental conditions must assure that the documenet will not become wet or dirty so as to cause extraneous marks or damage. Operator training in marking the document must be given, and operator consistency must be dependable. Suitable forms must be designed and available. Moreover, greater time is required, since the source documents normally are transported to a central facility for reading and processing. Finally, optical mark reading presents a relatively high error rate, due to character or mark rejections or substitutions.

There is thus a great need for what may be termed an electronic notebook, i.e., a device which has the flexibility and adaptability of receiving and storing the entered data but which avoids the entry of erroneous data and facilitates instead entry of correct data. The device moreover must be capable of rapid and accurate readout of the data for subsequent storage and/or processing and avoiding manual conversion.

In general, any process where data is collected manually in the field and later entered into a computer, is a potential application for the present invention. The term "electronic notebook" concisely describes the range of applications.

SUMMARY OF THE INVENTION

The present invention overcomes these and other inadequacies and deficiencies of prior art systems, and offers an economical and accurate means of performing data gathering operations and entering the gathered data into a computer without the necessity of additional human operations. Particularly, the present invention provides for simplified and highly efficient gathering of data, even in remote locations, and includes a hand-held, portable keyboard-to-memory data terminal for collecting data in the field and electronically storing the data in an efficient manner for later read-out. An interface-formatter provides for automatic conversion of the data to a format which is computer compatible, and suitable for transmission directly to a computer and/or for local print-out of a hard copy

of the data as well as local storage (e.g., magnetic tape).

In a preferred embodiment, numeric data is entered into the collection device by a keyboard. A large amount of storage is provided in the collection device to permit its use over a desired duration, e.g. a day or longer, whereupon the data stored in the data collection device must be retrieved and the device cleared for further collection purposes. A significant aspect of the read-out from the collection device into the interface-formatter is that manual transcription and formatting are eliminated, thus avoiding such costly functions as manual compilation, transcription, keypunching and verification as are involved in the typical prior art systems. The present invention may be viewed as a general purpose data entry system applicable to a broad range of industries and applications.

The present system satisfies a need for data collection and input, both for end users with in-house computers and for time-shared computer users, and for communications in the computer industry in general — i.e., the need of speeding up data entry.

More particularly, the data collection device is a hand-held, battery powered, keyboard-to-memory device for entering and storing numeric source data for later transmission to a computer. Source data is entered manually by actuating keys of a keyboard. The data is stored in a solid state memory and simultaneously displayed via a light emitting diode display where it can be checked for accuracy. If an error is detected in an entry, the erroneous data is easily erased and re-entered, by character. Subsequent data is entered in the same fashion.

During data collection, the display can be used to view the entire contents of memory, line by line, showing previously entered data, and blanks where no data has been entered. Simple operator controls allow the entry of a character anywhere in memory. The memory is like a page of a notebook — the entire page can be viewed, and data can be added, erased, or corrected anywhere on the page, and all before the "page" is submitted to the computer.

The display shows the line number (0 to 99) and the data corresponding to that line. The number of characters in a line is programmable, up to 32. The line can be broken into four fields or less, programmable to conform to the format of data collection. Each field can be up to nine characters. Thus, similar to designing a paper form with blanks to fill in, the display can be programmed to correspond to a desired format of data collection. Programming is done via a read-only-memory (ROM) diode matrix at the factory to customer specification, and differently programmed ROM's may be substituted in the field.

On the display, a pointer shows where the next character will be entered in a line. The pointer can be moved back and forth across a line, similar to forward spacing or backspacing a typewriter, to enter a character at any location on the line. The display can be rolled backward or forward through memory, line by line, with the data for the corresponding line and field showing. The field of interest on a particular line can be selected via the keyboard. The keyboard also allows a tab to be set, to set the pointer at a selected character location each time a line is rolled forward or backward, similar to the tab on a typewriter.

The dataholder memory can be pre-loaded from a computer or terminal to load selected fields of each line. The computer entered data can then be displayed or modified like keyboard entered data. Thus, fixed data can be carried to the field corresponding to the variable data to be collected.

At the end of a data collection period, the device is attached to a companion formatter which in turn is connected to a communication terminal. On command, the information held in memory is transmitted through the formatter, and into the communication terminal. The communication terminal may be a hard-copy type such as a teletypewriter, or simply a modem such as a dataphone.

The interface-formatter includes appropriate control circuits for interjecting SPACE's, carriage return (CR), and line feeds (LF), at preprogrammed positions in the output data stream. The interface-formatter as well provides the necessary conversion from the parallel character storage of main memory to a serial format for transmission. The formatter, in like manner, includes necessary counting and logic circuits for timing the bits in the output bit stream, for counting the characters in each line of data and determining in light of the accumulated count the positions in which to insert SPACE's, for detecting the count of each line and for counting the number of lines to determine the positons for inserting the CR, LF, and like characters.

The interface-formatter provides several output interfaces, for example, the transmission may be in ASCII code, bit serial, at selectable baud rates form 110 to 1200 baud.

The interface-formatter also provides an input interface to the electronic notebook for receiving transmission from the computer and converting the transmitted data into a form acceptable by the electronic notebook for storing in memory. Receipt of transmitted bit serial ASCII is provided by means of a serial receiver synchronized with the incoming data bit stream to accept and convert the serial bits to parallel-characters. The computer is programmed to transmit the data and controls in the format in which the intended receiving dataholder is programmed. Thus, the data and control signal inputs received from the computer transmission directly simulate the corresponding inputs produced by key actuation. Thus, the appropriate line and field shift control signals are transmitted for entering the "fixed data" into the appropriate preselected lines and fields of the data memory, to enter data in selected fields and lines of the memory.

Where hard copy of the source data must be generated before transmission to a computer, the formatter is capable of arranging the print-out by the hard copy terminal to be of a specified format such as a log scaling ticket, inventory report, or shipping/receiving report. The data remains in memory after the print-out for subsequent print-outs or transmission to a computer, and is cleared only on direct command.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A through 1D comprise schematics of, and FIG. 1E comprises a timing diagram for, the keyboard entry portion of the portable data gathering device of the invention;

FIGS. 2A through 2C, inclusive, comprise a schematic of, and FIG. 2D comprises a timing chart for facilitating an explanation of, the keyboard entry portion of the portable data gathering device of the invention;

FIGS. 3A, 3B and 3D comprise schematics of, and FIG. 3C comprises a timing chart for explanation of, circuits for responding to the control signals developed primarily by the control circuits in FIGS 2A through 2C for producing memory addressing signals and display enabling and control signals;

FIG. 4A illustrates the memory components and the addressing, enabling and control inputs and data input and output connections, of the portable dataholder device;

FIGS 4B and 4C illustrate the circuits providing communication between the dataholder device and the interface formatter.

FIGS 5A through 5F, inclusive, comprise circuit diagrams of the interface formatter.

FIGS. 6A and 6B comprise top and side views, the latter partially in cross section, of the structure of the portable dataholder device;

FIGS. 7A and 7B comprise top and side views of the structure of the interface formatter, and

FIG. 7C comprises an end view, partially in cross section, as to the interface formatter of the dataholder as physically received on the interface formatter for interconnection of the dataholder and the interface formatter.

DETAILED DESCRIPTION OF THE INVENTION

To facilitate an understanding of the detailed circuit schematics, it is convenient first to describe the organization of the memory and the nature of data entry into the memory.

The memory is of the solid state random access (RAM) type; it may be of any desired size, and as an exemplary embodiment, is disclosed as having a capacity of 32 lines, with 32 digit positions per line. Each line is divided into a number of fields, shown herein as a maximum of four fields, with a maximum number of characters per field, again illustratively shown herein to be nine. The only entries into memory are the source data items, i.e., in the present application, one of the digits 1 to 9 and 0, in addition to a clear code. Hence, a maximum packing density of the stored data is accomplished, the necessary identifying and control digits being generated and inserted at proper positions in the data stream as the memory is subsequently read out by appropriate control circuits to be described.

As before noted, the portable device affords the functions of a true electronic notebook. As implied thereby, every digit or character position in each field of each line, and each line of plurality of lines, is selectively addressable by a number of different techniques or operating modes designed to simulate normal human entry operations in the source data collection while maximizing efficiency and accuracy. The fields of each line therefore correspond to different columns of a data collection sheet wherein similar information, for example, as to each of a number of different items, would be entered in each such column. It is to recognized, however, that the memory itself is not organized into fields but only into lines — the entry of data and its display, however, are performed in relation to the field organization of each line.

These functions will be more readily appreciated by a brief reference to FIG. 6A which illustrates the portable data collection device 1000. There is provided a keyboard having 16 individually actuatable keys including the numerics 0 through 9, cursor control 1013 having the upward and downward vertical arrows provide for advancing the display forward or moving it backward line by line for each depression or for automatic continuous rolling forward or backward for continued depression. The buttons 1016 and 1017 having horizontal arrows pointed to the left and the right comprise the cursor control, each depression moving the cursor correspondingly to the left or right by one position to change the location of a digit entry. The cursor affords a tab setting function, each new character being entered at the position at which the cursor is set; the cursor may maintain the tab setting for successive line changes, as well. The C button 1014 has a dual function, one being to clear the position currently indicated by the cursor. The D button is the field display control and changes the field shown on the display; moreover, holding the D button down for 1 second provides automatic scan of the memory, thereafter terminated by depressing the clear C button (i.e., the second of its dual functions). The display 1002 shows the line number and the corresponding data for that line and field. The cursor is displayed to indicate the next digit entry position, i.e., that to the left of the cursor. The cursor moves automatically for each digit entry and, as noted, can be moved independently by the cursor control buttons 1016 and 1017, and automatically tabbed.

The display 1002 includes two digit positions, 1020 and 1021, identifying the number of a line being displayed, a field indicator 1003, and nine character positions of data. The field indicator 1003 more specifically includes a top element 1003*a* which is illuminated to indicate that the first field is currently available, either for data entry or that data currently being displayed is from that field, and a second, bottom element 1003*b* providing the same indication, as to the second field. The top indicator 1003*a* is made to blink to indicate the third field and the bottom indicator 1003*b*, when blinking, similarly indicates the fourth field. A cursor indicator 1005 is provided at each digit position and when illuminated indicates the digit position currently available for data entry, erasure, or re-entry. For correction, a digit may be entered directly, automatically erasing the previous digit entry. The decimal point indicator of a standard numeric display element conveniently affords the cursor indicator. Moreoever, when battery power is low, the cursor indicators at all digit positions blink continuously.

In operation, and in a manner to be described, the device is initiated to place a blank or clear code into all positons in memory. Line 1 and field position 1 are made available and the cursor is automatically positioned for the first digit position. As each new digit is entered, the cursor automatically advances to the successive digit position. The cursor also can be moved under direct control, and without modifying existing data, by means of the cursor control buttons.

In a particular application of the device wherein it is desired to enter only two fields of data per line in a normal operation, when the first field is completed and the control button D depressed, the system advances automatically to the second successive field. If the segmented or open field button 1001 has also been depressed, the two additional fields are opened and depression of the button D then serves to advance to each of the third and fourth fields. Those extra fields are closed again for each new line advance.

into memory, until the new field is made available by depressing D. Further, when the last field (either field 2 or field 4) is completed, the forward key 1013 must be depressed to advance to a new line — i.e., further actuation of D will result only in recycling to the first field of the line. For an automatic scan operation, the button D is depressed for a longer preset period of approximately 1 second, resulting in the device automatically scanning through all fields in succession for each line in succession. Automatic scan is terminated by depressing the C button.

The segmented mode of operation facilitates the man-machine interface in that the operator must intentionally advance into the open field mode as an overt act, in the absence of which the device blocks further data entries when the pre-programmed number of fields in a given line are completed.

The buttons 1013 and 1012 provide for advancing through memory in a corresponding forward or backward direction, line by line, for each depression or for automatically and continuously advancing if the corresponding button is continuously depressed. The same corresponding field in each successive line is displayed in this operation. The line by line advance or backward scan from memory terminates upon release of the key; continued depression of the backward key returns the memory to the first line, i.e., line 01.

In light of this general discussion of the organization of the memory and the input controls in the data collection device, reference is now had to the detailed schematics of the device and initially FIGS. 1A through 1D which show the schematics, and FIG. 1E which shows a timing diagram for the keyboard entry portion of the device.

In FIG. 1A, the keyboard 100 includes sixteen switch contacts, corresponding to the 16 numeric and control input keys of the device. The switches are connected to corresponding outputs of a 4-line to 16-line decoder 101 which scans, or enables, the 16 switch contacts of the keyboard in sequence. Decoder 101 is driven by the 4 bit binary output of binary counter 102, which receives a 100 μ sec. pulse train from NAND gate 122. Decoder 101 thus performs a 16 bit time multiplex scan of the key switches; for example, if key 9 is depressed, the contact closure will be detected at the nine count of counter 102.

When a key is depressed, logic 1 on the keyboard common line 101*a* operates through inverter 113, and NAND 115 to set flip-flop 117, which in turn sets flip-flop 119. There results a 0 disabling input to NAND 122, and the 100 μ sec. pulse train no longer increments binary counter 102. Binary counter 102 thereby is latched at the binary count corresponding to the activated key as long as the selected key remains depressed. The count, and its complement, are also produced at the outputs of inverters 109 through 112 and at the outputs of NOR gates 103 through 106, respectively. The 100 μ sec. pulse is inverted by NOR gate 108 to trigger one-shot 107 in order to shift the output of binary counter 102 to the output of decoder 101 at a time when the output of counter 102 is not in a transient condition. Thus, it will be seen that the binary counter 102 is latched at an output 4 bit binary output value corresponding to the key which has been depressed. These four bits are provided as the bits A through D and their complements. The inputs E_A through E_D to NOR gates 103 to 106 are external 4-bit entries made through a connector on the unit simulating the binary code from counter 102: ESTRK is an external pulse simulating the DSTRK pulse. These external inputs provide for pre-loading the memory with fixed data which, of course, may be displayed and in relation to which corresponding source data can later be entered.

The foregoing functions are illustrated in FIG. 1E. At some random time in the count cycle, key 9 is depressed, the resulting steady state pulse typically being preceded by transient pulses due to switch bounce. When the binary output of counter 102 reaches a 9 count, i.e., A $\overline{B}$ $\overline{C}$ D, the resulting logic 1 output on the 9 line from decoder 101 results in setting of flip-flop 117 to produce the KEYDOWN pulse and setting of flip-flop 119 to produce the DSTRK pulse thereby disabling NAND gate 122 and terminating the train of binary CNTRCLK pulses. When the key is released, the output of NAND gate 115 falls to 0. The next occurring 1 to 0 transition of the 1.6 m sec. pulse train, through inverter 116, resets flip-flop 117 and terminates the KEYDOWN pulse. The next occurring 1 to 0 transition of the 1.6m sec. pulse train, through NAND gate 118, resets flip-flop 119 thereby terminating the DSTRK pulse. In FIG. 1A, $\overline{DSTRK}$ thus becomes logic 1 to enable NAND 122 to resume gating the binary CNTRCLK to counter 102 to resume the count. Thus, a DSTRK pulse is produced for each data entry and is maintained throughout the duration of key depression and for a time of at least 1.6 m sec. following key release. The 1.6 m sec. time period allows the maximum bounce time of the contacts, 1.0 m sec., to be logically filtered out.

The C (Clear) button results in a clear code 0101 ($\overline{A}$ B $\overline{C}$ D) for writing into memory at the currently available digit position. However, when RST (reset) exists, as automatically provided at initial power-on for a period in excess of the memory cycle time (409.6 m sec.), NAND 114 detects RST and C and latches counter 102 to the "clear" code thereby entering 0101 into all locations in memory.

FIG. 1B shows the circuits for translating the 4-bit counter code outputs generated in response to actuation of the control keys, to specific function lines. For example, when the left cursor pushbutton on keyboard 100 is activated, a 0010 code is produced at the output of binary counter 102. This code is detected by NAND gate 123 to produce an LSHFT pulse at the output of NOR gate 127 if DA = SA and $\overline{DSTRK}$ are both zero. As will be explained, a ROM, e.g. a diode matrix read-only memory, is pre-programmed for each data holder device to define the start address (SA) and end address (EA) for each of the four fields of each line, in common as to all lines. For convenience, a 4-bit binary code identifies these start and end addresses, permitting a total of 16 digit positions for two fields; a further signal termed "2nd 16" may be programmed for a given line to provide 32 characters instead of 16. The digit address (DA) in each field therefore must fall within the SA and EA for that field.

Accordingly, NOR gate 127 generates LSHFT for each $\overline{DSTRK}$ as long as DA does not equal SA. When DA equals SA, the digit address has returned to the start address, the equality of the input DA = SA is true producing a logic 1 which disables NOR gate 127 and terminates further generation of LSHFT pulses to prevent the cursor from being shifted off the left edge of the display. The similar observations hold as to generation of RSHFT pulses by NOR gate 128 in relation to

the condition DA = EA, i.e. to prevennt the cursor from being shifted off the right edge of the display.

Additional function signals are produced by logic decoding NOR gates 124 through 126, NOR gates 128 through 130, NAND gates 131 and 135, and NOR gates 132 and 136, as shown. With the exception of the CLR signal, inhibiting means prevent the codes for the special signals from being entered into memory. The outputs of NAND gates 123 through 126 are connected to the input of NAND gate 133. Thus, whenever one of the control keys is activated, the output of NAND gate 133 will be 1, thereby producing a 0 at the INHBT STROBE output of NOR gate 134. Similarly, actuating the D pushbutton produces 0 at the output of NAND gate 131 and a 1 at the FLDSHFT output of NOR gate 132 (if DSTRB is 0) and 0 at the INHBT STROBE output of NOR gate 134. Inverters 143 and 144 invert LSHFT and BSHFT respectively.

To accomplish the forward and back line "roll" or scan through memory, the corresponding forward-shift or back-shift key is pressed for longer than 819.2 m sec.; corresponding to the decoded outputs of NAND gates 125 and 126, supplied through NAND gate 137 to NAND 138, the latter also receiving the 819.2 m sec. clock, result in setting flip-flop 139, thereby enabling NAND gates 140 and 141. The 102.4 m sec. clock pulse train, through NAND gate 141 and inverter 142 produces a series of FSHFT (i. e., line forward shift) pulses at the output of NOR gate 129, each incrementing the memory address by one line. Thus, whereas momentary depression of the forward shift key advances one line, holding it down for 819.2 m sec. or longer causes the memory address to advance one line every 102.4 m sec. for as long as the forward shift key is held down. Alternatively, if BSHFT is 1 for 819.2 m sec. or longer, NAND 140 is disabled by the set output of flip-flop 139 and outputs a 0 for BSHFTDLY which remains as long as the back-shift key is depressed. For each BSHFT pulse, the memory address will be decremented one line. If the back-shift key is depressed for at least 819.2 m sec., a negative-going BSHFTDLY delay pulse will cause the memory address to be reset back to line 01.

If the D pushbutton is depressed, a FLDSHIFT pulse occurs to advance to the next data field. If the last data field in a given line is being accessed when D is pressed, the system merely cycles back to the first data field in the same line (advance to a successive line requires instead, actuation of the forward line shift button). Depressing D for longer than 819.2 m sec. alternatively places the data holder in the automatic scan mode.

The oscillator and timing circuits are contained in FIG. 1C. Oscillator 145 produces a 100 m sec. pulse train which is divided down by counters 146 and 147. The 25.6 m sec. pulse train from the output of counter 147 is inverted by inverter 148 and toggles flip-flop 149 to produce a 51.2 m sec. pulse train which is inverted by inverter 150 to toggle flip-flop 151 to produce a 102.4 m sec. pulse train. The 51.2 m sec. pulse train is also divided by counter 152 whenever any of the inputs to NOR gate 153 rises to 1. The 819.2 m sec. output from counter 152 is inverted by inverter 154 to toggle flip-flop 155 to produce a 1638.4 m sec. pulse train. Counter 152 and flip-flop 155 thus function as a gated oscillator.

The initial reset circuitry and the synchronizers for writing data into memory are found in FIG. 1D. The initial reset circuitry is used to reset the line and digit counters to the first memory location, reset the tabulators, and to fill the entire memory with a clear code (0101). In this regard, it is noted that clearing the entire memory is performed by at least momentarily turning off the system power, thereby to activate the reset circuits. At power-up, the voltage at the base of transistor 166 is initially 0, and through inverter 169, sets flip-flop 171 thereby making RST 1. Capacitor 168 begins to charge through resistor 175, and when the voltage reaches the transition level of inverter 169, its output falls to 0, thereby placing a 1 at the K input to flip-flop 171. On the next 0 to 1 transition of the 409.6 m sec. pulse train, flip-flop 171 is reset. The negative-going transition at the Q output of flip-flop 171 is coupled to inverter 174 to produce the RSTEND pulse. Flip-flop 171 thus outputs RST for at least 409.6 m sec. prior to RSTEND thereby to allow sufficient time for the memory to be cycled through each address and a CLEAR code (0101) to be written into each memory location.

In FIG. 1A, RST enables NAND gate 114; thus, at the time of the C output of decoder 101, the output of NAND gate 114 falls to 0, thereby producing a 1 at the output of NAND gate 115 to set flip-flop 117. Thus, binary counter 102 is locked at the clear code for the duration of RST.

In FIG. 1D, RST also enables NAND 156 to pass the 100 μ sec. pulse train and produce an RST $\overline{OSC}$ pulse train. The RST $\overline{OSC}$ 100 μ sec. pulse train occurs during the entire RST cycle to enter the clear code into memory.

During data entry, all of the inputs to NAND gate 159 are normally 1. The 1 to 0 transition of the DSTRB pulse, which occurs when a data key is depressed, is coupled through capacitor 157 and gates 159 and 160 to trigger one-shot 161, and through OR gate 162 to trigger one-shot 163.

In FIG. 1D (see also the timing diagram of FIG. 1E), the ϕpulse from one-shot 161 lasts for 30 μ sec., while the ϕ_1 pulse from one-shot 163 lasts for 7 μ sec. The trailing edge of the ϕ_1 pulse triggers one-shot 165 through OR gate 164 to produce a 7 μ sec. ϕ_2 pulse. The ϕ_2 pulse is used to write data into memory. This same sequence also is produced whenever the EXT $\overline{STROBE}$ falls to 0, or when the $\overline{XFET}$ falls to 0 during transmission of data from the data holder to the formatter. EXT $\overline{STROBE}$ falls to 0 when the end of a line is reached, to output an end of line code to the formatter. An $\overline{XFET}$ pulse occurs each time the formatter transmits a FETCH pulse to the dataholder to request readout and transmission of a new data item (digit) from memory to the formatter — as described more fully later.

The ϕ, ϕ_1, ϕ_2 sequence also is triggered by a $\overline{SCAN}$ $\overline{OSC}$ pulse in order to display the data contained in memory in the automatic scan operation.

The memory has a capacity of 1024 characters. Each location in memory is defined by a 10-bit memory address (A_0 through A_8 and CS). The four least significant bits of the memory address (A_0, A_1, A_2 and A_3) and A_8 (2nd 16 bit) define the digit address while the remaining bits of the memory address (A_4, A_5, A_6, A_7, CS) define the line address. Thus, the memory has a capacity of 32 lines, with a maximum of 32 characters per line.

As noted, each line can contain either two or four data fields. In operation, when the last digit entry of a first field of a line is made, the D button must be de-

pressed to sequence to the next data field. At the end of data entry for the second field, the FWD button must be depressed to sequence to the next line, and the D button must be depressed to sequence back to the first field. Alternatively, if the segmented field (field open) switch is actuated, access is gained to the two additional fields and data entry, field advance and ultimately line advance at the end of the fourth field, are accomplished in the same manner as described above. If desired, all four fields can be made available in each line.

Recall that there are three display modes. In one mode, successive momentary actuations of the D button cause repetitive cycling through only the fields of a given line — normally only the first two fields but when the field open switch is activated, all four fields are scanned and displayed in succession. In a second mode, for any particular field selected for display, the roll forward and roll back operations display the corresponding field for each of the successively preceding or succeeding lines. In a third mode, the D button is depressed for more than 819.2 m sec., to display each of the four fields in succession, for each line in succession. In automatic read-in and storage through the connector, data entry and its display proceed typically in continuous fashion through the selected number of fields of each line of data, for the totality of the data and in accordance with its programmed format, as supplied.

The schematic of the control circuitry is shown in FIGS. 2A through 2C. Digit address counter 202 in FIG. 2A is a presettable binary up-down counter which establishes the digit position in a memory line at which data is to be added. Each time data is entered, the digit address increments up by one count via $\overline{DSTRK}$ through NOR 206 and NOR 208. The digit address also is incremented selectively up and down by the RSHFT and LSHFT (the cursor key) inputs, respectively, to NOR 205, supplied through NOR 207 (enabled by $\overline{\phi}$ = 0 during DSTRK from flip-flop 161, FIG. 1D) and NOR 208. $\overline{LSHFT}$, of 1 and 0 values, applied to the UP/D input of counter 202 controls incrementing or decrementing of the count, respectively. Thirty μ seconds after DSTRK, $\overline{\phi}$ returns to 1, and the resulting 0 to 1 transition at the output of NOR 208 then increments digit address counter 202.

NAND 204 prevents DSTRK from incrementing counter 202 under three conditions:

1. "$\overline{DA = EA}$" is 0: This means that the digit address is off the data field to the right and therefore the data field is full.
2. "$\overline{INHBT\ STRK}$": This indicates that the DSTRK is caused by a control key, and not a data or clear key. This signal is used to prevent the activation of a function key from incrementing digit address counter 202, and from entering the function code into memory.
3. During SCAN, $\overline{DSTRK}$ will not shift the digit address nor allow access to memory. This is because during the scan mode, data is read out of, but never entered into, memory.

These three conditions also determine when NOR 203 is enabled to produce MSTRB, which controls writing of data into memory.

If none of these conditions is present, the 7 μ sec. $\overline{\phi}_2$ pulse will enable NOR 203 to output a 7 μ sec. MSTRB pulse, to write data into the memory.

As later detailed, the "field" definition is very flexible, in that the SA and EA of adjacent fields are essentially independent of each other, i.e., with respect to memory positions, fields may be immediately adjacent with the EA of one directly contiguous the SA of the next, or may be spaced, or may overlap. In the latter case, selected digits (to the extent of overlap) may be displayed both as the concluding digits of one field and as the initial digits of the next.

During read-out of data from the dataholder by the formatter, described in more detail hereafter, the formatter sends a FETCH pulse to request a new character of data to be transmitted, in response to which the dataholder produces XFET. The dataholder then generates XFET* for each XFET, and thus each FETCH, except at the beginning of a new data line, correspondingly to increment digit address counter 202 through NOR 208. XFET* is not generated during the FETCH which occurs at the beginning of a new line to permit the dataholder to transmit an end of line code or tag (a 4-bit word 0111) to the formatter to generate an end of line sequence CR (carriage return), LF (line feed), RO_1, RO_2 (rub-outs 1 and 2), before a new line of data is read out.

In FIG. 2B, the first character flip-flop 249 controls generation of XFET*, as described. It is set during transmission, or during reset, after the last data field of a line has been selected by the select controller 265. The field end flip-flop 262 detects the next selection after the last programmed data field in a given line and resets the select controller 265 and sets the first character flip-flop 249. For example, during read-out, normally SEL4 at the output of select controller 265 is the last field. When SEL5 becomes 1, field end flip-flop 262 is set through inverter 259 and NAND gate 260. With the field end flip-flop 262 set, SEL occurs simultaneously, and through NAND gate 263 outputs a negative-going pulse which, through NAND 264, resets select controller 265 to SEL1 and, if RST or XMIT is detected by NOR 245, through NOR 246, sets first character flip-flop 249. This disables NOR 252 and inhibits the XFET* pulse. The next occurring FETCH pulse produces a $\overline{XFET}$ pulse, applied through NAND 247 and inverter 248 to an input of NOR 252; however, NOR 252 is disabled by the 1 output of the now set, first character flip-flop 249, and thus no XFET* output results. This then affords the time for the end of line sequence, above described.

On the trailing edge of the said next occurring $\overline{XFET}$ pulse, the 0 to 1 transition at the output of inverter 248 resets first character flip-flop 249 and NOR 252 is again enabled. Subsequent $\overline{XFET}$ pulses then produce corresponding XFET* pulses through NOR 252 to increment digit address counter 202.

During the reset cycle, the $\overline{RSTOSC}$ pulse train passes through NOR 247, inverter 248 and NOR 252 to produce a series of XFET* pulses to cycle the memory through all address locations and write the clear code (0101) into each location.

The select controller 265 is a binary counter which activates its 8-line outputs sequentially for successive input pulses. It selects the data field shown on the display by its control inputs to the diode matrix ROM 214, which has pre-programmed therein start address codes SA_1, SA_2, SA_3, SA_4 and end address codes EA_1, EA_2, EA_3, EA_4 for the corresponding fields. Select controller 265 also is reset through NAND gate 264 at the start of a transmission when the $\overline{XMIT}$* pulse occurs or at the end of reset when the $\overline{RSTEND}$ pulse occurs.

At the beginning of transmission and at the end of reset, the digit address counter 202 and line address counters 401 to 404 (FIG 3A) are also reset. Thus, at the beginning of transmission and at the end of reset, the first digit position of the first data field in the first line is available for read-out or data entry.

The memory is normally cycled through 16 positions in accordance with inputs RA_1 to RA_4 (see FIG. 2A) to a 4 pole switch 224 which normally connects those inputs to its outputs, A_0, A_1, A_2, A_3, which are supplied to the digit address lines to the memory (see FIG 4C). The display is turned on only during a portion of the 16 position cycle. That portion can be as large as 9 digit positions, or as small as 1 digit position. The display is turned on when the Recirculate Address (RA) is equal to the Start Address (SA) via the array of exclusive OR gates 284 to 287 (FIG. 2C). This causes the Display flip-flop 295 to latch to ST DISP. When RA = EA (End Address) the Display flip-flop 295 is turned off, which turns off the display. (See FIGS. 2D and 3C). Whereas the RA inputs define a currently addressed digit position in normal cycling operations, a specific digit position defined by the digit address counter may be selected for data entry or clearing in accordance with switching switch 224 to the DA_1 to DA_4 inputs. 224 is switched by ϕ which is generated during the ϕ, ϕ_1, ϕ_2 sequence described previously.

Thus, the display shows only the digits corresponding to the selected field. Furthermore, only the selected field can be operated upon by the keyboard; the other digit positions in memory are not accessible without changing fields or lines. There can be up to 4 fields to a line of data, each field with a different number of digits. The programming of the fields is accomplished by the Diode Matrix ROM 214 which can be unplugged in the field and a differently programmed ROM inserted. Each ROM is programmed to a desired display format analogous to a desired format of lines and columns of a blank, form or tabulation sheet to be filled in, as in a paper notebook — thus, the analogy of the present invention to an electronic notebook.

Considering the foregoing in more detail, whenever the D pushbutton on keyboard 100 is pressed, a FLDSHFT pulse occurs which changes the field shown in the display. This pulse is inverted by inverter 236 and passes through NAND gate 243 to increment Select Controller 265. Flip-flop 244 is set to increment the select controller 265 during SMIT or RST (detected by NOR 245) and when DA=EA, which signals the end of a field; thus, during read-out (XMIT) the select controller is incremented to the next field upon completion of read-out of a preceding field, and during reset (RST) upon completion of resetting a preceding field. Flip-flop 244 is reset on the trailing edge of either $\overline{XFET}$ or $\overline{RSTOSC}$, through NAND gate 247 and inverter 248.

NOR 235 produces an $\overline{INCRLA}$ signal to increment the line address counter (FIG. 3A). The $\overline{INCRLA}$ signal can be produced in two ways: automatically, at the end of the last field if in XMIT or RST; or, by means of the FWD or BKWD keys 1012 and 1013, which cause FSHFT and BSHFT, respectively. If field end flip-flop 262 is set, upon occurrence of SEL, NAND gate 263 produces a signal to NOR 234, which transmits a signal to NOR 235 producing an $\overline{INCRLA}$ if FLDSHFT is false. If FLDSHFT is true, the signal from NOR 234 is inhibited. Thus, an $\overline{INCRLA}$ cannot be produced if FLDSHFT is true, which means that depressing the D key causes cycling through the fields on a single line; the line cannot be changed by the D key. The second way of producing an $\overline{INCRLA}$ is by depressing the FWD or BKWD keys 1012 and 1013 which supplies FSHFT or BSHFT, respectively, to NOR 225. NOR 225 produces a signal through INV 230 which is differentiated by RC 231 and 232 to cause NOR 235 to produce an $\overline{INCRLA}$ pulse.

Digit address counter 202 is preset selectively to either the SA or TA address the outputs of a 4-pole switch 201, by the DGTRST input. The DGTRST signal causes the DIGIT ADDRESS counter to assume the TAB address (TA), each time the FWD or BKWD key is depressed, and to assume the start address (SA) each time the field is changed. The DIGIT ADDRESS locates the cursor on the display and locates the address in memory for data entry or read out. The DGTRST signal occurs during the ϕ_1 pulse if either NOR gate 226 is enabled by FSHFT or BSHFT being detected by NOR gate 225, or NOR gate 227 is enabled by the occurrence of a select controller increment signal at the output of inverter 266 (FIG. 2B). However, when FSHFT or BSHFT is detected by NOR 225, a $\overline{PRESET}$ signal is sent to the 4-pole switch 201 (FIG. 2A) through inverter 200 to switch the outputs of the 4-pole switch from the start address (SA) to the TAB address (TA). Thus, each time a new data field is selected by activating the D key, the digit address (DA) 202 will be set to the start address (SA) as programmed and stored in diode matrix ROM 214, and each time the FWD or BKWD key is depressed, the DA 202 will be set to the TAB address.

At the start of transmission, a $\overline{XMIT}$* pulse is produced and at the end of the reset sequence a $\overline{RSTEND}$ pulse is produced. If either of these signals is detected by NAND gate 253 (FIG. 2B), a TABRST signal is generated which resets the tab address (TA) flip-flops 210 through 213 (FIG. 2A) and sets the digit address counter 202 to zero. The tab address (TA) moreover is set to the digit address (DA) each time a LSHFT, RSHFT, or FLDSHFT signal is detected by NOR gate 209. This means that each time the cursor is moved left or right via the LEFT or RIGHT shift cursor keys, the TAB address (TA) is set to DIGIT ADDRESS (DA); thus, the cursor comes up at the last position set by the LSHFT or RSHFT keys 1016 and 1017, each time the line is changed via FWD or BKWD keys 1012 and 1013, respectively. This allows the operator to position the cursor, much like setting the tab in a typewriter, to a desired position at which it remains for successive lines. Additionally, each time a new field is selected, the TAB address assumes the DIGIT ADDRESS which is the start address (SA) of the new field. Thus, the TAB is cleared each time the field is changed to keep the cursor from getting lost in another field upon line change.

The dataholder can be placed in a scan mode by holding the D pushbutton on keyboard 100 depressed. During the scan mode, the select controller 265 is automatically incremented to display each field of each line, in succession — such as for verification prior to transmission, or any other desired purpose. When the D pushbutton is held depressed, the FLDSHFT signal is produced and, through inverter 236 and NAND 243, increments the select controller 265. If D is held depressed longer than 819.2 m sec., NOR 239 is enabled on the trailing edge of the concurrent 819.2 m sec. pulse, coupled thereto through capacitor 237, to set the scan flip-flop 241. When flip-flop 241 is set, and the

CLR pushbutton is not depressed, NAND gate 242 is enabled so that the 1638.4 m sec. pulse train passes through NAND gate 242 to the input of NAND gate 243. However, as long as the D key is depressed the output of inverter 236 will be 0 disabling NAND gate 243. When the D key is released, NAND gate 243 will transmit the 1638.4 m sec. pulse train to increment select controller 265. This incrementing pulse also is coupled through inverter 266 to NOR 227 to produce, through NOR 228 and inverter 229, a DGTRST pulse. This pulse sets the digit address (DA) of digit address counter 202, through switch 201, to the start address at the output of diode matrix 214, for each new field, and thus each time the field is changed. Thus, as select controller 265 is incremented once every 1638.4 m sec., the digit address is set to the new start address derived from the ROM 214.

At the end of the last field, the Field End FF 262 is set via SEL 5 through inverter 259 and NAND 260 to enable NAND 263. NOR 267 generates SEL upon ϕ and SCAN OSC, and SEL in turn is transmitted through the enabled NAND 263 through NOR 234 and through NOR 235 to produce $\overline{\text{INCR LA}}$. NOR 234 is enabled only when FLDSHFT is not true. Thus, at the end of the last field, when not caused by FLDSHFT, the line counter is automatically incremented to the next line (during SCAN, RST, and XMIT, but not when the D key is depressed.)

The scan mode is terminated by momentarily depressing the CLR pushbutton, which operates through inverter 240 to disable NAND gate 242, and the 0 to 1 transition at its release operating through the inverter 240 to reset the scan flip-flop 241 and thereby disable NAND gate 242.

The dataholder normally utilizes two data fields. As mentioned earlier, field open flip-flop 257 normally is reset and enables NAND gate 258 so that when SEL3 is produced following completion of two fields, field end flip-flop 262 is set through NAND gate 260. However, if four fields are desired, the open field switch 255 of FIG. 2B (button 1001 in FIG. 6A) is depressed, which operates through NAND gate 256 to set the open field flip-flop 257 and disable NAND gate 258. SEL3 therefore is blocked by NAND 258, and field end flip-flop 262 remains set until SEL5, through inverter 259, is detected by NAND gate 260. Thus, when the open field switch is pressed, the field end flip-flop 262 will not be set until select controller 265 has incremented through four data fields. When the FWD or BKWD key thereafter is depressed to change lines, $\overline{\text{INCRLA}}$ at the output of NOR 235 resets open field flip-flop 257. Thus, the open field switch opens the two additonal fields for only one line at a time; each time the line is changed, the extra fields are closed, and only two are available normally. The field open flip-flop 257 is also reset, initially, by RSTEND. The alternative of having all fields always available is apparent.

The open field flip-flop 257 also is set during SCAN, XMIT, or RST by the corresponding inputs to NAND 256, to make the additonal fields available during each of these operations; in contrast to the momentary contact input of the open field switch 255, the signal inputs to NAND 256 are steady state and override the $\overline{\text{INCRLA}}$ reset function whereby the extra fields remain open for successive lines.

The field indicator 1003 (FIG. 6A) is activated by circuits of FIG. 2C. SEL1 disables NOR 270 and through inverter 271 activates transistor 273 to illuminate the top light emitting diode 275 (1003*a*). Similarly, SEL 2 causes illumination of the bottom light emitting diode 283 (1003*b*). If the open field switch 255 is activated to select two additional data fields, SEL 3 enables NAND 268 to pass the 51.2 m sec. pulse train for energizing the top light emitting diode 275 to blink on and off every 52.2 m sec.; similarly, SEL 4 causes blinking illumination of the bottom light emitting diode 283.

The outputs, A_0, A_1, A_2 and A_3, of 4-pole switch 224 normally are set to the RA_1 through RA_4 (Recirculate Address) inputs which continuously cycle through the 16 addresses of a line. FIG. 2D shows the signals from the timing circuits of FIG. 1C which are employed to generate RA_1 to RA_4 and also the relationship of the data positions of a field, as defined by SA to EA for an illustrative field — both as to the displayed field and correspondingly the digit positions of the field available for data entry or read-out. It will be recalled that the diode matrix ROM 214 provides a "2nd 16" output. "2nd 16" simply acts as one of the memory address bits (A_4) to allow access to those memory locations requiring the A_4 bit when in certain fields. The A_4 bit controls one-half of the memory, thus one-half of the memory is reserved for those fields programmed for "2nd 16". This allows a single line to have access to another 16 digits while using the same 4 bit (A_0, A_1, A_2, A_3) memory code for addressing a digit in a line.

When data is read into memory, ϕ (FIG. 1D) pulse causes the 4-pole switch 224 (FIG. 2A) to present the address specified by the digit address counter 202 to memory for the 30 microsecond duration of ϕ. During ϕ, ϕ_2 occurs to generate MSTRB at the output of NOR 203 (FIG. 2A) to write data held by the keyboard binary counter 102 into the memory location specified by the digit address counter.

The circuits which identify the decimal point indicator at the digit positions, to be illuminated as the cursor in the display, are also shown in FIG. 2C. Exclusive OR gates 297 through 300 and NOR gates 301 comprise a coincidence detector to produce RA = DA when the recirculate address equal the digit address.

FIG. 2C also shows the circuits which control the digit position shift functions through each field. Exclusive OR gates 302 through 305 and NOR gate 306 comprise a coincidence detector for DA = EA and, through inverter 307, $\overline{\text{DA = EA}}$. When DA = EA, data entry is inhibited and RSHFT is inhibited (FIG. 1B) to prevent the cursor from being shifted off the right of the display. This signal also sets flip-flop 244 (FIG. 2B) when in RST or XMIT, automatically to increment the select controller 265 at the end of each field during reset or read-out. Exclusive OR gates 308 through 311 and NOR gate 312 comprise a coincidence detector for DA = SA. When DA = SA, LSHFT is inhibited (FIG. 1B) to keep the cursor from moving off the left side of the display.

The foregoing has described the cycling through digit positions and fields of memory, as well as the generation of $\overline{\text{INCRLA}}$ to advance or return through successive lines of memory, and the various scan modes in which line advance or return (line shift) is performed. The circuits for responding to these signals and performing the requisite line selection functions are shown in FIG. 3A.

It will be recalled that the addressed digit positions in a given field are defined by A_0 to A_3 at the outputs of 4-pole switch 224 in FIG. 2A, as a function of succes-

sive DSTRB pulses produced by key actuation (resulting in the ϕ sequence) and timing signals producing RA_1 to RA_2 or in any of the scan or transmit modes (in which the digit address counter produces $\overline{DA_1}$ to DA_4). The line count, however, is defined by addresses A_4 to A_7 and C_1. Binary counter 401, at its outputs A_4 to A_7, counts 16 lines (0 to 15) and counter 402 outputs C_1 as the next (fifth) binary digit to afford a total line count of 32 (0 to 31). The next count resulting from $\overline{INCRLA}$ (effecting a 100000 count) results in the output (on line 402*a*) which sets the flip-flop of NOR gates 405 and 406 to reset the line count to line 01.

Although 32 lines are thus provided, more lines of memory, of course, could be implemented. The C_1 output is treated separately since it serves to select between two banks of memories — and thus is optional, as a function of the memories employed (to be discussed in FIGS. 4A and 4B). The line select ROM 214 of FIG. 2A will be recalled to produce a "2nd 16" output. That output is encoded by inverter 401*a* in FIG 3A to produce the A_8 output. This output provides for a 32 digit line (instead of 16 — not to be confused with the "open field" operation affording two additional fields per line) by calling up an additional 16 digit positions into the memory cycle for a given line, for certain pre-programmed fields (i.e., pre-programmed by ROM 214).

Thus, the binary outputs of counters 401 and 402, are the line address inputs to memory.

The BCD counters 403 and 404, however, provide 4-bit binary outputs identifying the units (U_1 to U_4) and tens (T_1 to T_4) digits of the line count, for purposes of display.

The binary counters 401 and 402 and BCD counters 403 and 404 are preset to line 01 through NAND gate 400 at the start of the transmit sequence when $\overline{XMIT}^*$ falls to 0, at the end of the reset sequence when $\overline{RSTEND}$ falls to 0, or when the back shift key is held down for longer than 819.2 m sec. causing the $\overline{BSHFTDLY}$ line to fall to 0. The counters are also reset when the maximum line count is reached, through the flip-flop formed by NAND gates 405 and 406 and inverter 405*a*. The counters are incremented by each $\overline{INCRLA}$ pulse in a direction determined by $\overline{BSHFT}$. Following reset by the flip-flop, the next $\overline{INCRLA}$ applied to the counters to resume their count also resets the flip-flop.

A "zero" count of counters 401 and 402 is detected by elements 407, 408 and 408*a* to produce BSHFT INHIBIT which prevents additional BSHFT pulses from occurring from the output of NOR gate 130 (FIG. 1B), to prevent rolling backward past line zero.

The display circuitry is shown in FIG. 3B. Each time $\overline{ST\ DISP}$ falls to zero, digit counter 416 counts the 400μsec. pulses from inverter 415 and activates the output lines D1 through D8 in sequence. Following generation of D8, the next 400μsec. pulse from inverter 415 sets flip-flop 420 to the D8 value (logic 1) to generate D9, and D8 terminates. The next 400μsec. pulse then clocks flip-flop 420 to set to zero and D9 terminates. Thus, each time $\overline{ST\ DISP}$ goes to 0, nine successive output pulses D1 to D9 are produced at the 400μsec. clocking rate. These outputs are applied to corresponding ones of nine LED data displays to activate each display in synchronism with addressing of the nine (maximum) digit positions of a field currently addressed in memory.

Flip-flops 417 and 419, and NOR 418, control the timed energization of the line number display positions. Prior to ST DISP, flip-flop 419 is set by a 400μsec. clock pulse, producing a 0 output. At the start of the display, ST DISP rises to one and sets flip-flop 417, producing a 0 at the output of NOR gate 418. The output of flip-flop 419 remains 0 since both inputs are 0. Because of the propagation delays in the circuitry, signal transitions occur slightly after the transitions for the 400μsec. pulse train. Thus when ST DISP falls to 0, both inputs to NOR gate 418 are 0 and a TENSEN signal is produced. Since ST DISP is no longer 1, the next 0 to 1 transition on the output of inverter 425 clocks a 1 to the output of flip-flop 417. This causes the output of NOR gate 418 to fall to 0, thereby terminating the TENSEN signal. However, while the TENSEN signal is still present at the input to flip-flop 419, a 0 to 1 transition at the output of inverter 415 occurs thereby clocking a 1 to the outut of flip-flop 419 and producing the UNITSEN signal shortly thereafter. The next 0 to 1 transition at the output of inverter 415 clocks the 1 at the output of flip-flop 417 to the output of flip-flop 419, thereby terminating the UNITSEN signal. Thus, it can be seen that after ST DISP and at the conclusion of each display period, a TENSEN pulse and a UNITSEN pulse are produced in sequence to illuminate the tens and units indicators of the line number display, as shown in FIG. 3C.

The display illustratively comprises, for each digit position, a seven segment font of individually energizable light emitting diodes (LED's). Accordingly, a 7 segment decoder 440 outputs on 7 lines A* to G* suitable energizing signals for the corresponding segments. These outputs are applied in common to each display position, as denoted by the (*) and the appropriate display position is enabled in timed sequence with the application to decoder 440 of the corresponding digit display information as to line number and data.

Thus, as seen in FIG. 3B, 4-pole switch 438 normally supplies the digit data from memory on inputs X_4 to X_8 to decoder 440. Under control of each TENSEN and UNITSEN through NOR 435, switch 438 supplies the outputs of switch 437 to decoder 440 — the switch 437 in turn normally supplies the tens digit bits (T_1 to T_4) to switch 438 but, in response to UNITSEN instead supplies the units digit bits (U_1 to U_4) to switch 438, each for application to decoder 440.

Elements 409 through 412 (FIG. 3A) comprise the power control circuitry. To conserve power, mercury tilt switch 411 opens to turn off the display panel when the unit is disposed downwardly — a normal position when not in use. When the unit is tipped up, as one would hold the device when entering data, the display is energized. A replaceable, preferably rechargeable, external battery 409 serves to power the display, to trickle charge the internal battery, and, when connected, to power the logic. When the external battery 409 is disconnected for replacement, the smaller internal battery 410 powers the logic. The small internal battery 410 can supply the logic for several hours to allow for charging or recharging the external battery, thus making the memory essentially immune to battery discharge problems.

A battery low voltage detector 412 produces a pulsating $\overline{BATTLO}$ signal whenever the battery voltage falls below a predetermined value. NAND 414 detects $\overline{BATTLO}$ and the output of NAND 413, when the recirculation address is equal to the digit address (RA

= DA) and STDISP is 1 (the digit address is greater than the start address but below the end address) to produce dp^*. dp^* thus is steady. The output of NAND gate 414 will also be 1 whenever $\overline{BATTLO}$ is 0 indicating that the battery voltage has fallen below a predetermined value. Since the digit address is a steady state value and the recirculate address is rapidly changing, the decimal point for that digit will be turned on only for the display digit in which data is about to be entered. However, when the battery low signal is produced, all of the decimal points in the display will be illuminated by the pulsating $\overline{BATTLO}$ signal to produce a blinking effect.

The memory and output circuits are contained in FIGS. 4A and 4B. The memory for the A bit comprises registers 451 and 452, for the B bit, registers 453 and 454, for the C bit, registers 455 and 456, and for the D bit, registers 457 and 458. The memories are addressed in common by A_0 to A_4. In addition, C_5, the highest order bit of the line address, selects between memories 451, 453, 455 and 457 (C_5) and memories 452, 454, 456 and 458 ($\overline{C_5}$). During data entry, the dataholder is not connected to the formatter and thus $\overline{XCONN}$ is 1. NAND gate 450 thus is enabled by each 7μsec. MSTRB pulse to gate a 4-bit word (A to D) into the commonly addressed memory locations (line and digit position) of the corresponding memories A to D (in the set selected by C_5).

The data in memory, as addressed, is always available for read-out at X_A to X_D, and thus for simultaneous display during write-in (MSTRB = 1) or merely for display of stored data (MSTRB = 0) as well as for transmission, or read-out.

As previously noted, for transmission of the data from memory in the dataholder at the remote terminal, the dataholder is electrically connected to a corresponding connector of the interface-formatter. Preferably, this is accomplished simply by sliding the formatter into position to complete the electrical connection as shown further in FIGS. 6A and 6B. As illustrated, this automatically produces a CONNECT signal, although a separate switch could, of course, be provided. Data transmission then is initiated by depressing the forward shift key. The transmission automatically terminates when a clear code for an entire line of data is detected, or by activating the clear key.

In FIG. 4B, the CONNECT signal produces XCONN and, through inverter 473, $\overline{XCONN}$. As will be described, and as mentioned earlier, the interface-formatter sends a FETCH pulse to the dataholder to request each new character, FETCH producing $\overline{XFET}$ through inverter 472. $\overline{XCONN}$ and $\overline{\phi_2}$ are detected by NOR gate 483 to produce STRBOUT and, through inverter 484, $\overline{CONTREAD}$. Preferably each of the foregoing signals communicated between the dataholder and the interface-formatter as well are coupled through optical isolators (i.e., including as well $\overline{XMITOUT}$, XMIT*, etc.).

In FIG. 3D each seven segment LED digit 492a through 492k is driven in common at the anode connections by the outputs A* and G*, and dp^*, from seven segment decoder 440 and NAND 414. The cathode connection of each LED digit is driven respectively by transistors 491a through 491k. The transistors 491a through 491k are switched on respectively by the positive signals D1 through D9, TENS, and UNITS. Thus, each LED digit 492a through 492k is enabled in timed sequence with the outputs of seven segment decoder 440 and NAND 414 to display the corresponding digit information as to line number, data, and cursor position.

When the dataholder is so connected and the forward shift key is depressed, $\overline{XCONN}$ and FSHFT are both false, enabling NOR 465 and setting the flip-flop of NOR gates 466 and 467 to the transmit mode, producing XMIT and its complement. The one to zero transition at the output of NOR gate 467 is coupled through capacitor 468 to produce $\overline{XMIT}^*$ and, through inverter, 470, its complement $\overline{XMIT}^*$.

Referring to FIG 4C, the memory outputs X_A through X_D are supplied to corresponding gating circuits which, if enabled, produce the output bits A_{OUT} to D_{OUT} for transmission to the interface-formatter. Preferably optical isolators couple the logic gate outputs to the output terminals. As shown, the CONNECT signal enables the isolators 486 to 489. Assuming that a character presently read from memory as the signals X_A through X_D is not the first character of a new data line, the 1st CHAR flip-flop 249 of FIG. 2B is not set and thus the 1st CHAR input to each of NOR 475 and NAND 476 is false. $\overline{XCONN}$ is false and $\overline{\phi}$ is false (from FIG. 1E) since it is assumed that the system currently is in the 30μsec. address interval of ϕ. The enabled NOR 475 output is inverted twice through inverter 474 and NOR 475 for supply to isolator 486, for generation of A_{OUT}. Under the same assumptions, NAND 476 enables NAND gates 480 to 482 to pass the outputs of the corresponding NAND gates 477 to 479 which are likewise enabled by XCONN and ϕ. In accordance with the preceding assumptions, the memory outputs X_B to X_D, respectively, are doubly inverted and coupled to the corresponding isolators 487 to 489 to produce B_{OUT} to D_{OUT} respectively.

Where a character currently presented as X_A to X_D is the first of a new line, the 1st CHAR input is true and the logic gates are disabled. It will be recalled that under this condition, the digit address for the memory likewise is not advanced, so that the dataholder may transmit the end of line tag or code to the formatter which in turn generates the end of line sequence (CR, LF, RO_1 and RO_2).

The circuits of FIG. 4B generate the end of line tag 0111. NOR 475, in response to the true input 1st CHAR, supplies logic 0 as A_{OUT}; conversely, NAND 476, in response to 1st CHAR during ϕ, outputs logic 0 to NAND 480, 481 and 482 which in turn supply logic 1 as the outputs B_{OUT}, C_{OUT} and D_{OUT}.

The transmit mode is terminated, as previously noted, when the clear code is detected for an entire line of data. NOR gate 461 receives X_A and X_C directly and X_B and X_D through inverter 459 and 460. Recalling that the clear code is 0101, NOR gate 461 outputs logic 1 for each clear code detected in a digit position. NOR 462 therefore outputs 0 if for an entire line, no character other than the clear code is read from memory. This serves to maintain flip-flop 463 reset and thus outputting logic 0 to NOR 464. $\overline{XTRASTRB}$ at the set input to flip-flop 463 (produced by the 1st CHAR flip-flop 249 of FIG. 2B) becomes logic 0 when the 1st CHAR flip-flop 249 is reset thereby enabling NOR 464 to output NO DATA LINE to the flip-flop of NOR gates 466 and 467. This resets the flip-flop, ending the XMIT mode. Flip-flop 463 is reset by RST and thus normally outputs logic 1 to NOR 464.

The interface-formatter circuits are shown in FIGS. 5A through 5F.

131

means responsive to the start and end addresses of a selected field as established by said defining means for supplying the coded character signals from the storage positions of the memory for a selected line and field, as accessed by said accessing means, to said display means for display at corresponding display positions

42. A device as recited in claim 41 wherein said accessing means and said coded character signal supplying means operate in synchronism

43. A device as recited in claim 41 wherein the indication of an addressed line stored by said storing means comprises a numerical designation of that line relative to the total lines of memory and wherein:

said display further includes character display positions for displaying a line count equal to the maximum number of lines of said memory, and

said means for supplying coded character signals from the storage positions of a selected line and field, as accessed by said accessing means, further is responsive to, and supplies, the stored numeric indication of a selected line to the line count display positions of said display.

44. A device as recited in claim 40 wherein said means for storing an indication of a stored position address maintains the said stored position address for successive line shift control signals and thus for successively addressed lines, said addressing means thereby addressing and rendering available the corresponding position in each such successive line.

45. A device as recited in claim 40 wherein said display means further includes means associated with each character display position to provide a visual display indicating th stored position address thereby to identify the currently addressed position in memory.

46. A device as recited in claim 40 wherein said addressed position storing means is responsive to each field shift control signal to store the start position for that field, from said defining means, as the currently addressed position.

47. A device as recited in claim 46 wherein said addressed position storing means is responsive to each successively entered character data signal to advance the stored position address the next successive position of the selected field.

48. A device as recited in claim 40 wherein said keyboard includes a selectively actuable key and corresponding responsive means for producing forward and backward addressed position shift control signals, and said addressed position storing means is responsive to said addressed position shift control signals to shift the stored addressed position indication selectively forward and backward, respectively, through the data positions of a selected field.

49. A device as recited in claim 48 wherein said responsive means is controlled by the predetermined start and end addresses of selected field to inhibit shifting of the stored position beyond the said start and end addresses for a given field.

50. A device as recited in claim 39 wherein said line shift key actuation responsive means is responsive to said key actuation for less than a predetermined time, to produce a single line shift control signal, and to said key actuation in excess of said predetermined period of time to produce a continuing succession of line shift control signals.

51. A device as recited in claim 40 wherein said shift key actuation responsive means is responsive to said key actuation for less than a predetermined period of time to produce a single field shift control signal, and is responsive to said key actuation in excess of said predetermined period of time to produce a continuing succession of field shift control signals.

52. A device as recited in claim 51 wherein there is further provided means for accumulating a count corresponding to the number of successive field shift control signals and logic means responsive to successive such field shift control signals for advancing said count accumulating means and for recycling said count accumulating means at the maximum field number, thereby to address cyclically and in succession the fields of a currently addressed line, and alternately responsive to said continuing succession of field shift control signals for correspondingly advancing said count accumulating means and producing for each maximum field number count thereof a line shift control signal for shifting to a successive line, thereby to address in succession each field of each line

53. A device as recited in claim 40 wherein there are provided a first predetermined number of fields normally available in each line and an additional, second predetermined number of fields optionally available in each line and wherein there are further provided manually actuable means for rendering the said additional, second predetermined number of fields available during data entry operations.

54. A device as recited in claim 53 wherein, during read-out of said memory, each of said first and second predetermined number of fields is automatically rendered available in succession for successive field shift control signals during addressing of a given line of memory.

55. A device as recited in claim 39 wherein said keyboard includes a clearing control key and means operable in response to actuation thereof to enter a clear code as the character data code in an addressed position in memory.

56. A device as recited in claim 55 wherein there is further provided means responsive to initial turn-on of power of said device automatically to produce said clear code for a predetermined time interval following said power turn-on, and

said addressing means is operable during said predetermined time interval following power turn-on to address each successive position of each line in succession in memory, thereby to enter the clearing code in each addressable position of memory.

57. A device as recited in claim 39 for use with a read-out means to which said device is connected for reading out the data from said memory of said device for supply of the read-out data to the utilization means, and wherein said device further includes:

means operable when said device is connected to said read-out means to produce a connect signal for placing said device in a read-out and data transmit mode of operation, and

said addressing means is operable in said transmit mode of said device, in response to a line shift control signal, to address and read out each memory storage position in succession of each line, for all such lines in succession, of said memory.

58. A device as recited in claim 57 wherein said addressing means further includes means for recognizing the completion of addressing of the last storage position in a given line and the advance to the first storage position of a successive line to temporarily halt

138

FIG. 5A shows primarily the initiating controls and interfaces with the dataholder and a sequence generator which controls the rate of read-out of data from the dataholder and the sequence in which data bits are supplied in the output bit stream from the formatter.

As discussed in relation to FIGS. 4A–4C, when the dataholder is connected to the formatter and the forward shift button is depressed, XMIT*OUT is transmitted to the formatter and in FIG. 5A is applied through inverter 502 and effectively inverted by NAND 503 to set flip-flop 504. Flip-flops 504 and 505 were previously reset and thus flip-flop 505 presents logic 0 to NAND 506.

Transmit clock source 538 generates a selectable clocking rate of 10, 15 or 30 pulses per second to produce correspondingly a character per second transmission rate, and hence read-out rate, from the dataholder. On the transmit clock pulse next occurring after the setting of flip-flop 504, flip-flop 505 is set whereupon NAND 506 is enabled by two logic 1 inputs to supply through inverter 507 a clock pulse to counter 510. NAND gate 506 remains enabled for supply of the transmit clock pulses and counter 510 continues to count, generating a 4-bit BCD output *a, b, c, d* and their complements. These 4-bit outputs are decoded by NAND gates 526 through 535 to produce in sequence $\overline{STP\ 1}$, FETCH ?, $\overline{B1}$ through $\overline{B7}$, PAR and $\overline{INCREM}$. There is also a one shot space between FETCH and $\overline{B1}$ which is not decoded.

Counter 510 continues this cycling count through its 12 output conditions in synchronism with the transmit clock rate until conclusion of readout of the data from the dataholder. Particularly, when $\overline{XMIT\ OUT}$ becomes true, XMITTING, through inverter 515, becomes false and resets flip-flops 504 and 505. Through inverter 509, $\overline{XMITTING}$ becomes true and counter 510 is reset.

The data stored in the data holder may be arranged in blocks of any desired number of lines, if desired, by the simple provision of skipping a line of data entry and leaving a line blank. As described elsewhere herein, when the interface-formatter receives an entire line of clear codes, it terminates sending of further requests for more data, and thus the dataholder terminates read-out of data.

This permits, for example, removal of a billing ticket, or the like, printed at the remote terminal, and insertion of a new ticket to be printed. The dataholder is essentially in a standby mode in this instance, and by depression of the forward shift button, the transmit and read-out mode is established again to read-out the next block of data.

Organization of the stored data into blocks also permits use of header information for each block (as indeed it may be provided for any stored data) in accordance with an appropriate format, as desired, for which the system is programmed, for recognition and interpretation of the header as distinguished from data.

A separate header identification code may be employed in the present system in the alternative, through the provisions taught in the copending application of Azure Ser. No. 435,540, filed Jan. 22, 1974.

Note also that while XMITTING is true, transistor 521 is rendered conductive to energize LED 520 to indicate to the operator that transmission is occurring.

In FIG. 5B, the 4-bit parallel data lines AOUT to DOUT are connected to inputs of bistable latch 541. $\overline{CONTREAD}$ from FIG. 4B produced at ϕ_3 during "connection" is applied through inverter 539 to one shot 540 to set the outputs of latch 541 to its inputs. The resulting outputs ACONT through DCONT are applied to the inputs of bistable latch 542, which then is set at the trailing edge of the next occurring FETCH pulse, the latter also activating one shot 543 to generate $\overline{FETCHEND}$.

FETCH is generated by NAND 545 in response to the $\overline{FETCH?}$ decode output of counter 510 in conjunction with the negation of various logic conditions as shown, including the end of line sequence, and others. When none of these conditions exists, the $\overline{FETCH}$ output of NAND 545, through inverter 548, supplies FETCH to latch 542, thereby producing the outputs LATCH A through D and the complements of A through C, and through one shot 543, $\overline{FETCHEND}$. $\overline{FETCH}$, through inverter 546, activates transistor 547 to produce FETCH for transmission to the dataholder to select a further character for transmission to the interface-formatter.

NAND 537 responds to $\overline{LATCH\ A}$ and $\overline{LATCH\ C}$, and LATCH B and LATCH D and also $\overline{PROGSP}$ to produce SPACE; this corresponds to decoding the clear code 0101, previously discussed, to produce a space during printout or for transmission of a space code to a remote receiver.

The end of line sequence (C/R, L/F, RO_1, RO_2) occurs during XMITTING whenever FETCH and the 1st CHAR code which follows each data line (0111) is detected by NAND gate 549. The 1 to 0 transition at the output of NAND gate 549 is differentiated by capacitor 550 and resistor 551 (with parallel protective diode 552) to produce a negative going pulse that sets flip-flop 553. Upon the next FETCH? stage the 1 at the output of flip-flop 553 will be shifted to the output of flip-flop 554, and a 0 will be clocked to the output of flip-flop 553. Thereafter, the 1 will be shifted one flip-flop upon each succeeding FETCH? stage producing in sequence C/F, L/F, RO_1 and RO_2.

For a purpose to be described, the number of characters in each line and the number of lines are counted. Whereas the respective counters are shown in FIG. 5E, the count pulse inputs thereto are generated in FIG. 5B. Particularly, the set output from flip-flop 571, CHCNTR, is true for each character and the set output from flip-flop 575, LNCNTR, becomes true for each line.

Considering first flip-flop 571, it is reset during transmission of a character by $\overline{XMITTING}$ through inverter 570 and also when $\overline{INCREM}$ is 0 (through inverter 558 and NAND 564) and also when any of the end of line sequence conditions are true, or logic 1, i.e., L/F line, RO_1, RO_2 and C/R as applied through inverters 559–563, as indicated, to the inputs of NAND 564.

Where none of the special characters before noted is present, the normally zero output of NAND 567 switches to 1 in response to the INCREM pulse produced each time a character is transmitted in accordance with $\overline{INCREM}$ applied through inverter 559 to NAND 567. This requires that L/F line be zero thereby through inverter 566 producing a logic 1 to NAND 567, so that the logic 1 output therefrom is obtained on the trailing edge of INCREM.

In summary, one CLKIN pulse is produced for every INCREM pulse and thus each time a character is transmitted, and one $\overline{L/F*}$ pulse is generated for each L/F line pulse and CLKIN time a line feed is transmitted. The Q output of flip-flop 571 thus is set to 1 and the

one output of CHCNTR for each character thus is supplied to the character counter.

If either RO_1, RO_2 or C/R is 1, NAND gates 564 and 567 will be disabled to inhibit the production of either L/F* or CLK IN pulses. Thus, the end of record characters are not counted by the character counter.

Just prior to transmission XMITTING is 1 which, when inverted by inverter 573, places a 0 on the set input of flip-flop 575 to make its Q output initially 1. Whenever a L/F* signal is produced at the output of NAND gate 564 the 0 at the input to flip-flop 575 will be clocked to the Q output. Thus, the Q output of flip-flop 575 is initially set to 1 and the 1 is shifted through the line counter 700 by the L/F* pulses.

As noted, the counter 510 outputs establish the sequence and timing of the data and special character bits for transmission as a serial pulse train. In FIG. 5C, the four data bits, LATCH A to D, from latch 542 (FIG. 5B) are presented to normally enabled NAND gates 576 to 579 to produce BIT 1 to BIT 4, respectively. NAND gates 580 and 581 are tied to 1 inputs (+) and produce 0 outputs for BIT 6 and BIT 7 and NAND 582, tied to 0 (ground) produces a 1 as BIT 5, corresponding to the numeric portion of the ASCII code.

If any special character is present at the input to NAND gate 583, the resulting 1 output through inverter 584 becomes 0 and disables NAND gates 576 through 582, tending to bias all output lines to 1, i.e., for BIT 1 to BIT 7. However, the presence of one or more special characters, through selected matrix interconnections of inverters 585*a* through 594*g* and the output bit lines serves to clamp certain of the output lines to 0. The particular code for a given special character may be selected by simply wire wrapping the signal line for that character to the proper output line or lines. Thus, the interface-formatter can be made compatible with any of the standard teletype or computer formats such as ASCII or EBDIC. Using the configuration shown, for example, if L/F is present, L/F is 0 which, through NAND 583 and inverter 584, sets the outputs of NAND's 576 to 582 to 1. L/F at NAND 601 supplies 1 to inverters 585*a* to *f*, setting the outputs of inverters 587*a* through 587*f* to 0. Only inverters 585*c* and 585*d* are tied to their corresponding lines, i.e., BIT 3 and BIT 4. Thus, the parallel ASCII code for L/F is 1010111.

Parity circuit 600 receives BIT 1 to BIT 7 and produces in response thereto an error or an odd parity output.

Referring to FIG. 5D, the parallel ASCII output is converted to a 12 bit serial word. The serial bit time sequencing is afforded by the sequential, decoded outputs of counter 510 (FIG. 5A): STP1, FETCH?, B1, B2, B3, B4, B5, B6, B7, PAR and INCREM applied to NAND gates 616 to 624. Thus, for example, the output of NAND gate 616 is 1 for the first, second and twelfth bit times and otherwise 0. The outputs of NOR gates 617 through 623 at the fourth through tenth bit times (recall a space exists at time "three") corresponds to bits 1 through 7, respectively. Odd or even parity is selected by switch 624*a*, and supplied as its inverse through NAND 624 enabled by PAR. The NOR gate 616 to 624 outputs, through inverters 625 to 633, are joined at a common output line to produce SERIAL, and through inverter 634, SERIAL. The SERIAL output is 1, 1, 0 (Space), BIT 1, BIT 2, BIT 3, BIT 4, BIT 5, BIT 6, BIT 7, (even or odd) PARITY, and 1.

SERIAL may drive a teletype drive circuit, through inverter 605 and coupler 606. Darlington configured transistors 608 and 609 conduct for SERIAL at 0 and are off (or in low condition) for SERIAL at 1. Diodes 612, 613, 614 and 615 are provided to allow either TTY terminals to be biased with a positive voltage. Zener diode 610 is provided to clip the output voltage at a safe value when transistors 608 and 609 are in their off condition.

The circuits used for programming line feeds and spaces within the data stream as well as for generating a > LINE singal when a predetermined number of lines have been counted are found in FIGS. 5E and 5F.

A header may be and typically is provided for each block of data, and the dataholder can be programmed to accommodate any desired number of header lines, up to a maximum of nine, and each may be different in format. (The number 9 is simply a design choice and additional hardware could be provided to accommodate a greater number, if required.) In FIG. 5E, the line counter 700 counts the number of lines in each header. A 1 is placed at the LINE 0 input to shift register 700 at the start of transmission and at the beginning of each header. However, LNCNTR returns to 0 at the start of the first L/F* pulse. Thereafter, the 1 is shifted one stage for each L/F* pulse, and thus for each line feed, indicating the number of lines in a given header. At the start of each header, DETECT L is 0 and resets the line counter to zero.

The character counter 701 to 704 counts the number of characters in a given line. A 1 is placed on the CH0 input of shift register 701 at the start of each transmission and upon the occurrence of each L/F LINE pulse. However, CH CNTR returns to 0 at the start of the first CLK IN pulse. Thereafter, the 1 placed in the first stage of shift register 701 is shifted one stage for each CLK IN pulse. Since one CLK IN pulse occurs for each character transmitted, the position of the 1 is an indication of the number of characters that have been transmitted. The character counters 701 through 704 are reset to zero by CLEAR, which is 0 at the end of a transmission or whenever a line feed is transmitted.

The line counter 700 and character counter 701 through 704 (FIG. 5E) also are operative to interject spaces and line feeds in predetermined locations in the serial output. Appropriate character counter and line counter outputs are connected by wire wrap to the inputs of NAND gates 720 through 743 (FIG. 5F). The outputs of these NAND gates are connected by wire wrap to either the PROG SP terminals (the input of inverters 744, 746 and 748) or the PROG LF terminal. For example, to insert a space at line 2, character 10 of NAND gate 720 is connected at its inputs to the LINE 2 output of line counter 700 and to the CH 10 output of character counter 702. The output of NAND gate 720 is connected by wire wrap to the input of inverter 744. Thus, when line 2 character 10 is reached, the output of NAND gate 720 will fall to 0 and, after passing through inverters 744 and 745, will appear as a 0 on the PROG SP signal line.

Inverters 750 through 755 provide the capability of programming a wide variety of logic functions.

The portable dataholder device, or electronic notebook, is intended for hand-held operation and thus must be lightweight and portable, and operable under extreme environmental conditions. The arrangement of the keyboard and display on the upper surface of the device as shown in FIG. 6A has been discussed previ-

ously. With joint reference to FIG. 6B, the display area 1002 includes a recessed display screen 1004 for viewing the characters formed by the light emitting diodes 1006. Any of numerous types of electro-optical display elements may be employed, the elements 1006 being merely illustrative. Recall that a mercury switch energizes the display when the device is inclined toward a horizontal position, the recessed screen 1004 facilitating viewing even in bright daylight.

The data and control pushbuttons are flush with the upper surface of the housing 1000 to avoid inadvertent actuation. The necessary electronics are mounted on suitable circuit boards or other circuits, as suggested in FIG. 6B. A removable battery pack 1008 is carried on the back surface of the portable dataholder. A multiple contact connector 1010 carrying numerous electrical connections to the memory and control circuits of the dataholder is mounted for convenience on the rear of the housing. A protective cap on the connector may be provided or other precautions taken to insure hermetic sealing of the dataholder unit.

In the planar and side views of FIGS. 7A and 7B, the housing 1012 for the interface and formatter circuits includes an upper planar surface 1014 carrying 2 spaced apart vertical rails 1016 and 1018 and a connector 1020. FIG. 7C shows that the connector 1020 mates with the connector plug 1010 of the dataholder when the latter is received on the side rails, thereby to provide an automatic electrical connection between the dataholder and the formatter and interface circuits.

An on/off power switch 1022 and a suitable indicator 1024 may be provided. A local/line switch at 1026 selects between local print-out or transmission. A transmitting indicator 1028 corresponds to the light emitting diode 520 of FIG. 5A, for indicating data transmission.

In summary, the system of the invention achieves the desiderata of a true electronic notebook having greatly simplified data input operations with simultaneous display for verification. Connection of the dataholder to the interface/formatter circuit which may be at a remote station for communication to a central is of the utmost simplicity and the operation for reading out of the stored data requires actuation of essentially only a single switch, the data being read out in a format which is both computer-compatible and suitable for transmission, totally avoiding the need for keypunch or other intervening operations. A significant feature is that the system performs formatting independently of the dataholder device per se, simplifying its construction while maximizing the data packing density. The "wire-wrap"-programming of the formatter may be afforded in the alternative by a programmed diode matrix. Plural, differently programmed such matrices may be provided in a given formatter/interface unit, to be selected in accordance with the intended formatting of the information items collected in any of various different dataholders. Greater versatility of a given formatter thus is provided.

Whereas the stored data is not formatted per se, the diode matrix ROM (214) provides both for entry and display of data in accordance with the desired format. The ROM may be changed in the field for a different format.

The disclosed format includes two standard fields per line, with any desired number (up to 9) of characters per field (up to a maximum of 16 per line) and the availability of two additional such fields per line. Moreover, the ROM permits programming a second 16 characters per line. The maximum limits are arbitrary, of course, and may be altered as desired.

The operator may call up any field in any line, may tab a character entry position for each line, may enter or erase (clear) and re-enter a character at any desired position at random, and may scan the storage in a number of modes — e.g., line by line for a given field (similar to scanning a column of figures on a page), in forward or backward directions, or field by field in succession for all lines in succession.

A significant feature is the ability to enter fixed data into selected locations from an external source through the input-output connector, in relation to which fixed data variable (source) data thereafter is entered.

The automatic formatting during read-out either for local hard copy printout and/or for transmission is, of course, highly significant, eliminating human errors while greatly increasing speed of data collection and transmission. Moreover, data storage is retained for verification prior to, during and after read-out. The dataholder thus is a true electronic notebook.

Numerous modifications, adaptations and applications of the system of the invention will be apparent to those skilled in the art, and thus it is intended by the appended claims to cover all such modifications, adaptations and applications which fall within the true spirit and scope of the invention.

What is claimed is:

1. A self-contained, hand-held portable data collection device for receiving and storing character data for subsequent read-out and transmission of the character data in a desired format to a utilization means, comprising:

entry means for supplying coded signal representations of character data and controls, the character data coded signals to be stored in said device at addresses determined in accordance with control coded signals associated with the character data coded signals,

A random access memory having plural character data storage positions arranged in plural lines, each line including plural said storage positions,

means for addressing the memory in accordance with the control coded signals for entry and storage of the character data coded signals in an addressed position,

display means for visually displaying characters represented by character data coded signals,

output connection means,

said addressing means including means for selectively addressing said memory for reading out character data coded signals stored in positions of said memory and for selectively supplying said signals read out from said memory to said display means for display thereof, and to said output connection means to be available for transmission thereof to a utilization means, and

electrical energy storing means integral with said self-contained hand-held portable data collection device for supplying electrical energy to the aforesaid means for operation of the said device, said electrical energy storing means comprising:

first and second energy storing cells, and means connecting said first and second energy storing cells normally to enable said first cell to supply electrical energy as aforesaid and to permit depletion of substantially all electrical energy

154

stored in said first cell prior to depletion of the electrical energy stored in said second cell, said connecting means being responsive to depletion of the electrical energy stored in said first cell below a predetermined level, automatically to enable said second cell to supply energy to at least said memory means for maintaining storage of said coded signals theretofore entered and stored therein

2. A device as recited in claim 1 wherein said entry means comprises a keyboard having plural character select keys and plural control select keys, said character select keys being individually and selectively actuable for producing respectively corresponding character data coded signals and said control select keys including keys individually and selectively actuable for producing respectively corresponding control coded signals for selectively addressing said memory.

3. A data collection device as recited in claim 1 wherein said entry means comprises means for receiving externally supplied data and associated control coded signals, and

said addressing means is responsive to the externally supplied control coded signals and said externally supplied data coded signals for addressing said random access memory in accordance with said external, coded control signals and for entering and storing said externally supplied data coded signals in corresponding positions of said memory in accordance with said addressing thereof.

4. A device as recited in claim 1 wherein:

said memory includes means for continuously recirculating the contents of the storage positions of each line thereof, and

said selective supplying means supplies the character coded signals from at least selected ones of the storage positions of the line of said memory addressed by said selective addressing means, during said recirculation thereof, for display by said display means.

5. A device as recited in claim 4 wherein said addressing means includes means for accumulating a count corresponding to the line of a currently addressed position of the memory.

6. A device as recited in claim 5 wherein said display is responsive to the count of said accumulating means for displaying the number of the line currently addressed in accordance with that accumulated count.

7. A device as recited in claim 1 wherein there is further provided:

means defining a desired number of fields in each said line, each field comprising a pre-selected number of storage positions defined in accordance with predetermined start and end addresses out of the plurality of addressable storage positions of a line,

said entry means includes means for supplying line shift control signals to effect, selectively, forward and backward shifting through successive lines of the memory and field shift control signals for shifting to successive fields of a given line of the memory, thereby to select a line and field of the memory for data entry and read-out,

said addressing means being responsive to said line and field shift signals for correspondingly advancing to and addressing the selected line and field of the memory, and

said display means includes individual display elements corresponding to the storage positions of a field for displaying characters in accordance with the coded character signals stored in the positions of a selected, addressed field and line of said memory.

8. A device as recited in claim 7 wherein said addressing means further includes means for maintaining an indentification of a selected field, and said addressing means is responsive to each successive line shift control signal to advance to the corresponding field as identified by said field identification maintaining means in each such successive line

9. A device as recited in claim 8 wherein said addressing means further includes means for producing and storing a cursor identifying a currently addressed position of a given line, and is responsive to each successive line shift control signal to advance to a successive line and address the corresponding position thereof as identified by the stored cursor of said cursor storing means.

10. A device as recited in claim 9 wherein said display means further includes means associated with each character display position to provide a visual cursor indication and means for selectively energizing said cursor indication means in accordance with the position of said stored cursor to identify the currently addressed position in memory.

11. A device as recited in claim 9 wherein said addressing means includes means responsive to each field shift control signal to select the start position for that field as the initial addressed position for the field, said storing means storing the cursor to identify the said initial address position as the currently addressed position.

12. A device as recited in claim 11 wherein said cursor producing means is responsive to each successively entered character data signal to advance the cursor to the next successive position of the selected field.

13. A device as recited in claim 9 wherein said entry means includes means for supplying cursor forward and backward shift control signals, and said cursor producing means is responsive to said cursor shift control signals to shift the stored cursor position selectively forward and backward, respectively, through the data positions of a selected field.

14. A device as recited in claim 13 wherein said cursor producing means is responsive to the predetermined start and end addresses of a selected field to inhibit shifting of the cursor position beyond the said start and end addresses for a given field.

15. A device as recited in claim 7 wherein said entry means includes means for selectively supplying forward and backward line shift control signals for shifting through successive lines of said memory, and

said addressing means responds to said line shift control signals correspondingly to address the thus identified line of memory and a field preselected therein.

16. A device as recited in claim 15 wherein means for supplying line shift control signals comprises a manually actuable control key and means responsive to actuation thereof for less than a predetermined time, to produce a single line shift control signal, said addressing means responding thereto to shift to and address a corresponding, successive line of memory, said actuation responsive means further being operable upon actuation of said control key in excess of said predetermined period of time to produce a continuing succes-

sion of line shift control signals, and said addressing means responding to each of said continuing succession of line shift control signals, correspondingly to shift to and address successive lines of said memory.

17. A device as recited in claim 7 wherein said means for supplying field shift signals includes a manually actuable control key and means responsive to actuation thereof for less than a predetermined period of time to produce a single field shift control signal, said addressing means responding thereto to address the successive field of a given line, and responsive to actuation thereof in excess of said predetermined period of time to produce a continuing succession of field shift control signals, and said addressing means responds to said continuing succession of field shift control signals correspondingly to shift to and address each field in succession for all fields of all lines in memory.

18. A device as recited in claim 17 wherein said addressing means includes means for accumulating a count corresponding to the number of successive field shift control signals and logic means responsive to successive, single such field shift control signals for advancing and recycling said count accumulating means thereby to cyclically address in succession the fields of a currently addressed line and alternately responsive to said continuing succession of field shift control signals for correspondingly advancing said count accumulating means and producing for each maximum count thereof a line shift control signal for shifting to a successive line thereby to address in succession each field of each line.

19. A device as recited in claim 17 wherein there are provided a first predetermined number of fields normally available in each line and an additional, second predetermined number of fields optionally available in each line and wherein there are further provided manually actuable means for rendering the said additional, second predetermined number of fields available during data entry operations.

20. A device as recited in claim 19 wherein, during read-out of said memory, each of said first and second predetermined number of fields is automatically rendered available in succession for successive field shift control signals during addressing of a given line of memory.

21. A device as recited in claim 7 wherein there is further provided a visual display indicator to indicate a currently selected and displayed field of the plural fields of a line.

22. A device as recited in claim 7 wherein said field defining means comprises a programmed read only memory.

23. A device as recited in claim 7 wherein said addressing means includes means for accumulating a count corresponding to successive fields shift control signals for deriving from said field defining means the start and end addresses of a currently selected field, as identified by the said count.

24. A device as recited in claim 23 wherein said count accumulating means remains at an accumulated count for successive line shift signals, thereby to continue to select the corresponding field for each of successively selected lines.

25. A device as recited in claim 23 wherein said addressing means further includes logic means responsive to a predetermined number of field shift signals to recycle said count accumulating means.

26. A device as recited in claim 1 wherein said entry means includes a keyboard having plural character data keys and plural control keys, one of said control keys comprising a clearing control key operable to enter a clear code as a character data code in an addressed position in memory.

27. A device as recited in claim 26 wherein there is further provided means responsive to initial turn-on of power to said device automatically to produce said clear code for a predetermined time interval following said power turn-on, and

said addressing means is operable during said predetermined time interval following power turn-on to address each successive position of each line in succession in memory thereby to enter the clearing code in each addressable position of memory.

28. A device as recited in claim 1 for use with a read-out means to which said device is connected for reading out the data from said memory of said device for supply of the read-out data to the utilization means and wherein said device further includes:

means operable when said device is connected to said read-out means to produce a connect signal for placing said device in a read-out and data transmit mode of operation,

said entry means including means for supplying a line shift control signal, and

said addressing means is operable in said transmit mode of said device, in response to a line shift control signal, to address and read out each memory storage position in succession of each line, for all such lines in succession of said memory.

29. A device as recited in claim 28 wherein said addressing means further includes means for recognizing the completion of addressing of the last storage position in a given line and the advance to the first storage position of a successive line to temporarily halt the addressing of said first position of said successive line and to transmit an end of line code to said read-out means.

30. A device as recited in claim 29 wherein said read-out means, following receipt of each character data signal from said device, transmits a FETCH pulse to said device to request a further character data signal to be read out from the next successive storage position in said memory and wherein:

said addressing means responds to each such successive FETCH pulse to transmit the character data signal of the next successively addressed position in memory.

31. A device as recited in claim 30 wherein there are further provided:

means for automatically entering a clear code into each data storage position in memory prior to entry of character data, and wherein

said read-out means responds to receipt of the clear code for each position of an entire line of memory thereby to terminate the transmission of further FETCH pulses to said device.

32. A device as recited in claim 30 wherein:

said entry means includes means for entering a header symbol control signal in an addressed line of memory thereby to identify successive line of character data stored in memory as a related block of data and,

said read-out means responds to receipt of the header symbol as read out and transmitted thereto by said device to terminate temporarily the further transmission of FETCH pulses to said device.

33. A device as recited in claim 32, further comprising

means for re-initiating read-out and transmission of character data from said memory following said temporary termination, thereby to provide for read-out and transmission to, and receipt by said read-out means of the character data of each block thereof stored in said memory, in individual succession as to each of a plurality of such blocks stored in memory.

34. A device for use with read-out means as recited in claim 29 wherein said read-out means responds to each end of line code received from said device to generate an end of line sequence.

35. A device for use with read-out means as recited in claim 28 wherein said read-out means further comprises

formatting means for responding to the character data read from each position in memory to convert the said data into a serial bit stream including coding and control bits for transmission to said further utilization means.

36. A device for use with read-out means as recited in claim 28 wherein said read-out means further includes means for receiving and transmitting to said device fixed character data and related control signals, and said addressing means of said device is responsive thereto to address the line and positions of memory in accordance with the received control signals for entry of the fixed character data into the corresponding, said addressed positions of memory.

37. A device for use with read-out means as recited in claim 28 wherein said read-out means further comprises formatting means for establishing a format of the data read from said memory of said device corresponding to the format of the data as entered into said device by said entry means thereby to control said utilization means to reproduce the transmitted character data in the format by which said character data was entered.

38. A device for use with read-out means as recited in claim 37 wherein said utilization means comprises a printer responsive to the output signals of said read-out means for printing a hard copy of the character data read out from said memory of said device in accordance with the format of that data as entered into memory.

39. A self-contained, hand-held portable data collection device for receiving and storing character data for subsequent read-out and transmission of the character data in a desired format to a utilization means, comprising:

a keyboard having a plurality of selectively actuatable character data and control keys,

means responsive to key actuation to produce corresponding character data and control coded signals,

a random access memory having plural character data storage positions arranged in plural lines, each line including plural said storage positions,

first means for storing an indication of each position of a line of memory, as addressed,

means responsive to each character data signal produced by key actuation to advance the addressed position indication of said storing means to a successive position,

said keyboard including selectively actuatable forward and backward line shift keys and said key actuation responsive means responding to actuation thereof to produce corresponding forward and backward line shift control signals,

second means for storing an indication of each line address of memory, and responsive to each line shift control signal to shift, in corresponding forward and backward directions, the line address indication as stored therein to a successive line,

addressing means responsive to the stored line and position indications of the respective storing means therefor, for addressing the thus identified position and line to render that position available for data storage,

means for entering character data signals corresponding to an actuated key in a currently addressed position of the memory,

display means for displaying a character corresponding to the character signals stored in at least a currently addressed memory position, and

electrical energy storing means integral with said self-contained hand-held portable data collection device for supplying electrical energy to the aforesaid means for operation of the said device, said electrical energy storing means comprising

first and second energy storing cells, and means connecting said first an second energy storing cells normally to enable said first cell to supply electrical energy as aforesaid and to permit depletion of substantially all electrical energy stored in said first cell prior to depletion of the electrical energy stored in said second cell, said connecting means being responsive to depletion of the electrical energy stored in said first cell below a predetermined level, automatically to enable said second cell to supply energy to at least said memory means for maintaining storage of said coded signals theretofore entered and stored therein.

40. A device as recited in claim 39 wherein there is further provided:

means defining a desired number of fields in each said line, each field comprising a pre-selected number of storage positions defined in accordance with predetermined start and end addresses out of the plurality of addressable memory positions of a line,

said keyboard further includes a field shift control key selectively actuable to select a next successive field,

said means responsive to key actuation includes means to produce a field shift control signal in response to each said field shift control key actuation, and there is further provided,

means for storing an indication of a selected field, and said means being responsive to each field shift control signal to correspondingly shift the stored indication of the selected field to a successive such field.

41. A device as recited in claim 40 wherein there is further provided:

means for successively accessing all positions of a selected line of memory in a continuously recirculating cycle,

said display means includes individual display positions corresponding to the maximum number of storage positions of a field, each display position displaying a character in accordance with the coded character signals stored in a position of the memory, and

the addressing of said first position of said successive line and to transmit an end of line code to said read-out means.

59. A device as recited in claim 58 wherein

said read-out means, following receipt of each character data signal from said device, transmits a FETCH pulse to said device to request a further character data signal to be read out from the next successive storage position in said memory, and

said addressing means responds to each such successive FETCH pulse to transmit the character data signal of the next successively addressed position in memory.

60. A device as recited in claim 59 wherein there are further provided

means for automatically entering a clear code into each data storage position in memory prior to entry of character data, and wherein

said read-out means responds to receipt of the clear code for each position of an entire line of memory thereby to terminate the transmission of further FETCH pulses to said device.

61. A device as recited in claim 57 wherein:

said entry means includes means for entering a header symbol control signal in an addressed line of memory thereby to identify successive lines of character data stored in memory as a related block of data, and

said read-out means responds to receipt of the header symbol as read out and transmitted thereto by said device to terminate temporarily the further transmission of FETCH pulses to said device.

62. A device as recited in claim 61, further comprising:

means for re-initiating read-out and transmission of character data from said memory following said temporary termination, thereby to provide for read-out and transmission to, and receipt by, said read-out means of the character data of each block thereof stored in said memory, in individual succession as to each of a plurality of such blocks stored in memory.

63. A device for use with read-out means as recited in claim 58 wherein said read-out means responds to each end of line code received from said device to generate an end of line sequence.

64. A device for use with read-out means as recited in claim 57 wherein said read-out means further comprises

formatting means for responding to the character data read from each position in memory to convert the said data into a serial bit stream including coding and control bits for transmission to said further utilization means.

65. A device for use with read-out means as recited in claim 57 wherein said read-out means further includes means for receiving and transmitting to said device fixed character data and related control signals, and said addressing means of said device is responsive thereto to address the line and positions of memory in accordance with the received character data and related control signals for entry of the fixed character data into the thereby addressed, corresponding positions of the memory.

66. A device for use with read-out means as recited in claim 57 wherein said read-out means further comprises formatting means for establishing a format of the data read from said memory of said device corresponding to the format of the data as entered into said device by said entry means, thereby to control said utilization means to reproduce the transmitted character data in the format in which said character data was entered.

67. A device for use with read-out means as recited in claim 66 wherein said utilization means comprises a printer responsive to the output signals of said read-out means for printing a hard copy of the character data read out from said memory of said device in accordance with the format of that data as entered into memory.

68. A device as recited in claim 1 wherein said electrical energy storing means further comprises means for detecting the depletion of electrical energy in said first cell below said predetermined level to provide an indication of such depletion.

69. A device as recited in claim 68 wherein said detecting and indicating means comprises means for producing a pulsating electrical output to provide a pulsating electrical energy depletion indication.

70. A device as recited in claim 69 wherein said detecting and indicating means comprises:

means for producing a pulsating electrical output, and

means for supplying said pulsating electrical output to said display means to provide a pulsating visual display as said electrical energy depletion indication.

71. A device as recited in claim 1 wherein:

said connecting means connects said first cell and said second cell to permit charging of said second cell by said first cell while normally enabling said first cell to supply electrical energy, and to prevent charging of said first cell by said second cell upon enabling said second cell to supply electrical energy at least to said memory.

72. A device as recited in claim 1 wherein:

said first cell is replaceable, and

said connecting means enables said second cell to supply energy to at least said memory means for maintaining storage of said coded signals entered and stored therein during removal of said first cell.

73. A self-contained, hand-held portable data collection device for receiving and storing character data for subsequent read-out and transmission of the character data in a desired format to a utilization means, comprising:

entry means for supplying coded signal representations of character data and controls, the character data coded signals to be stored in said device at addresses determined in accordance with control coded signals associated with the character data coded signals,

a random access memory having plural character data storage positions arranged in plural lines, each line including plural said storage positions,

means for continuously recirculating the contents of the storage positions of each line of said memory,

means for addressing the memory in accordance with the control coded signals for entry and storage of character data coded signals in addressed positions of said memory,

display means for visually displaying characters represented by character data coded signals,

output connection means,

said addressing means including means for selectively addressing each line of said memory for supplying at least selected ones of the coded signals of corre-

sponding, selected storage positions of the addressed line during said recirculation of the contents of the storage positions of the line, to said display means for display thereby, and to said output connection means to be available for transmission thereof to a utilization means, and

electrical energy storing means integral with said self-contained hand-held portable data collection device for supplying electrical energy to the aforesaid means for operation of the said device,

said addressing means includes counter means for accumulating a count in accordance with an addressed line of said memory, and

said supplying means supplies said count of said count accumulation means along with said at least selected ones of the recirculating coded signals of the addressed line of said memory to said display means for display of the line number in association with the characters defined by the said at least selected ones of the coded signals of that addressed line, and to said output connection means to be available for transmission thereof to a utilization means, thereby to identify the line of the coded signals as displayed and as available for transmission.

74. A device as recited in claim 73 for use with a read-out means to which said device is connected for reading out the data from said memory of said device for supply of the read-out data to the utilization means, and wherein said device further includes

means operable when said device is connected to said read-out means to produce a connect signal for placing said device in a read-out and data transmit mode of operation, and

said addressing means is operable in said transmit mode of said device, to address and read-out, in succession, the coded signals of the successive memory storage positions of each line, in succession for plural such lines of said memory for supply to said output connection means, and

said read-out means is operable to read out and transmit the count of said count accumulation means in association with the succession of coded signals of the successive storage positions of the line of said memory addressed in accordance with the count of said count accumulation means, for each successive count and the corresponding successive line of said memory.

* * * * *

CHAPTER 30 — PRIOR ART CITATIONS TO OFFICE AND REEXAMINATION OF PATENTS

Sec.

301. Citation of prior art.
302. Request for reexamination.
303. Determination of issue by Commissioner.
304. Reexamination order by Commissioner.
305. Conduct of reexamination proceedings.
306. Appeal.
307. Certificate of patentability, unpatentability, and claim cancellation.

§ 301. Citation of prior art

Any person at any time may cite to the Office in writing prior art consisting of patents or printed publications which that person believes to have a bearing on the patentability of any claim of a particular patent. If the person explains in writing the pertinency and manner of applying such prior art to at least one claim of the patent, the citation of such prior art and the explanation thereof will become a part of the official file of the patent. At the written request of the person citing the prior art, his or her identity will be excluded from the patent file and kept confidential. (Added December 12, 1980, Public Law 96-517, sec. 1, 94 Stat. 3015.)

§ 302. Request for reexamination

Any person at any time may file a request for reexamination by the Office of any claim of a patent on the basis of any prior art cited under the provisions of section 301 of this title. The request must be in writing and must be accompanied by payment of a reexamination fee established by the Commissioner of Patents pursuant to the provisions of section 41 of this title. The request must set forth the pertinency and manner applying cited prior art to every claim for which reexamination is requested. Unless the requesting person is the owner of the patent, the Commissioner promptly will send a copy of the request to the owner of record of the patent. (Added December 12, 1980, Public Law 96-517, sec. 1, 94 Stat. 3015.)

§ 303. Determination of issue by Commissioner

(a) Within three months following the filing of a request for reexamination under the provisions of section 302 of this title, the Commissioner will determine whether a substantial new question of patentability affecting any claim of the patent concerned is raised by the request, with or without consideration of other patents or printed publications. On his own initiative, and any time, the Commissioner may determine whether a substantial new question of patentability is raised by patents and publications discovered by him or cited under the provisions of section 301 of this title.

(b) A record of the Commissioner's determination under subsection (a) of this section will be placed in the official file of the patent, and a copy promptly will be given or mailed to the owner of record of the patent and to the person requesting reexamination, if any.

(c) A determination by the Commissioner pursuant to subsection (a) of this section that no substantial new question of patentability has been raised will be final and nonappealable. Upon such a determination, the Commissioner may refund a portion of the reexamination fee required under section 302 of this title. (Added December 12, 1980, Public Law 96-517, sec. 1, 94 Stat. 3015.)

§ 304. Reexamination order by Commissioner

If, in a determination made under the provisions of subsection 303(a) of this title, the Commissioner finds that a substantial new question of patentability affecting any claim of a patent is raised, the determination will include an order for reexamination of the patent for resolution of the question. The patent owner will be given a reasonable period, not less than two months from the date a copy of the determination is given or mailed to him, within which he may file a statement on such question, including any amendment to his patent and new claim or claims he may wish to propose, for consideration in the reexamination. If the patent owner files such a statement, he promptly will serve a copy of it on the person who has requested reexamination under the provisions of section 302 of this title. Within a period of two months from the date of service, that person may file and have considered in the reexamination a reply to any statement filed by the patent owner. That person promptly will serve on the patent owner a copy of any reply filed. (Added December 12, 1980, Public Law 96-517, sec. 1, 94 Stat. 3016.)

§ 305. Conduct of reexamination proceedings

After the times for filing the statement and reply provided for by section 304 of this title have expired, reexamination will be conducted according to the procedures established for initial examination under the provisions of sections 132 and 133 of this title. In any reexamination proceeding under this chapter, the patent owner will be permitted to propose any amendment to his patent and a new claim or claims thereto, in order to distinguish the invention as claimed from the prior art cited under the provisions of section 301 of this title, or in response to a decision adverse to the patentability of a claim of a patent. No proposed amended or new claim enlarging the scope of a claim of the patent will be permitted in a reexamination proceeding under this chapter. All reexamination proceedings under this section, including any appeal to the Board of Patent Appeals and Interferences, will be conducted with special dispatch within the Office. (Added December 12, 1980, Public Law 96-517, sec. 1, 94 Stat. 3016; Amended November 8, 1984, Public Law 98-622, Sec. 204 (c), 98 Stat. 3388.)

§ 306. Appeal

The patent owner involved in a reexamination proceeding under this chapter may appeal under the provisions of section 134 of this title, and may seek court review under the provisions of sections 141 to 145 of this title, with respect to any decision adverse to the patentability of any original or proposed amended or new claim of the patent. (Added December 12, 1980, Public Law 96-517, sec. 1, 94 Stat. 3016.)

§ 307. Certificate of patentability, unpatentability, and claim cancellation

(a) In a reexamination proceeding under this chapter, when the time for appeal has expired or any appeal proceeding has terminated, the Commissioner will issue and publish a certificate canceling any claim of the patent finally determined to be unpatentable, confirming any claim of the patent determined to be patentable, and incorporating in the patent any proposed amended or new claim determined to be patentable.

(b) Any proposed amended or new claim determined to be patentable and incorporated into a patent following a reexamination proceeding will have the same effect as that specified in section 252 of this title for reissued patents on the right of any person who made, purchased, or used anything patented by such proposed amended or new claim, or who made substantial preparation for the same, prior to issuance of a certificate under the provisions of subsection (a) of this section. (Added December 12, 1980, Public Law 96-517, sec. 1, 94 Stat. 3016.)

AFFIDAVIT

BIAGIO F. AMBROSIO, being sworn states as follows:

1. That he received an Electrical Engineering Degree from the University of Michigan in 1937 and has worked in the computer art from 1939 until the present time with extensive employment including IT&T and IBM. He considers himself a person skilled in the computer art and he considers that he was possessed of this skill before and after September 30, 1974, which was the filing date of his patent application on a Point of Action Billing Transactor which issued into United States patent No. 3,932,730 on January 13, 1976.

2. That at the filing of the application of Patent No. 3,932,730 on Spetmeber 30, 1974, he had knowledge of the computer concepts of ROM (read only memory) and RAM (random access memory), but that it was not obvious to him at that time that these concepts would have any utility in his invention other than as referred to in his patent.

B.F.A. 2/17/83

3. That his appreciation of the ROM and RAM concepts in the fall of 1976 was no greater than at the time he filed his patent application in 1974.

Biagio F. Ambrosio

Biagio F. Ambrosio

STATE OF CALIFORNIA :
: ss
COUNTY OF Los Angeles :

On this 17 day of February, 1983, before me a Notary Public, appeared BIAGIO F. AMBROSIO, to me personally known and did sign the above document as his free and voluntary act.

OFFICIAL SEAL
MONA PERNICK
NOTARY PUBLIC-CALIFORNIA
LOS ANGELES COUNTY
My Commission Expires July 1, 1985

Mona Pernick
Notary Public

AFFIDAVIT

MICHAEL T. GRAY, being sworn, states as follows:

1. He is 50 years of age and resides at 16501 Mozart Avenue, Los Gatos, California.

2. That his educational and employment experience comprise the following:

A. Education.

B.S. Physics
California Institute of Technology

B. Work Experience.

Scantlin Electronics 1957-1965 - Project Manager

Raytheon Learning Systems 1965-1967 - Chief Engineer

Gray Associates 1967-1968 - Managing Partner

Cybercom Corporation 1968-1971 - Vice President Engineering

Gray Computer Systems Corp., 1971-1976 - President

Lexar Corporation 1976-1978 - Program Manager Telecommunications Products

Anderson Jackson/Calcomp 1978-1980 - Manager, Telecommunications Division

Zitel Corporation 1980-1982 - Vice President Research and Development

3. That he is presently the owner of Gray Associates which are consulting specialists in man/machine interface; telecommunications; and microprocessor systems. Past product design programs of Gray Associates have included the following:

A. Display systems design including both CRT and flat panel displays.

B. Microprocessor systems design and applications including both hardware and software design. Products developed include systems based on the following microprocessors: 8086, 8088, Z80, 6800, 8080, 6502, 8008, and PPS4.

C. Telephone system design including:

Digital PABX design featuring both TDM and space switching technologies.

Voice digitization and synthesis using PCM and ADM technologies.

Integrated voice/data systems.

Computer simulation of network traffic handling.

D. Data communications systems including:

Communications interface design.

Protocols.

Error detection and correction.

Modems.

Secure communications.

E. Medical electronic systems including:

Medical data terminals.

Patient monitoring systems.

Microprocessor based clinical instruments.

F. Custom software development.

Gray associates also develops and presents technology training programs which have included the following:

Digital PABX design for integrated voice/data systems.

Communications interfaces and protocols.

CRT terminal systems design.

Introduction to microprocessor systems design.

Comparative analysis of 8 bit microprocessors.

4. That he has read and examined the following United States patents:

INVENTOR	PATENT NO.
Etter	4,133,034
Ambrosio	3,932,730
Lowell	4,115,870
Azure	4,016,542
Jones	3,956,740

5. That in the fall of 1976, based upon his knowledge of the technology of that time, he believes that one having ordinary skill in the art as exemplified by Ambrosio would have been more likely to have been led first to the teachings of Jones; and secondly to Lowell, and not to Azure, for the following reasons:

A. The Azure device is a hardwired discrete logic based portable entry terminal with keypad, display, RAM storage and a communications interface. Hardwired discrete logic was based on technology that was obsolete at that time. A microprocessor would have been the preferred approach.

B. Both the Jones and Lowell patents disclose microprocessor based devices which in 1976 would have pre-

sented a more logical modification of Ambrosio than would the hardwired discrete logic based portable entry terminal of Azure.

C. From a technical point of view, the Lowell disclosure offers no information or teaching that is not also apparent from the Jones patent. Further, from strictly technical considerations, the Etter device is more like the Jones device than either the Azure or Lowell devices.

D. While Jones does not allude to the use of his device for meter reading, and Lowell and Azure mention this usage, he believes that one having ordinary skill in 1976 would just as logically have been led to Jones as to Lowell or Azure upon being appraised of Ambrosio, because one of ordinary skill in the art of Ambrosio, if seeking to update the Ambrosio concept, and if having the insight to look to the existing microprocessor art of that time, would have appreciated that the Jones device would have been at least equally pertinent to the solution as Lowell and Azure would be. Ambrosio taught the utility meter reading concept, so since that application was already established by Ambrosio, any embellishment of Ambrosio in 1976 by one skilled in the art would have been towards what new microprocessor technology would improve Ambrosio. The fact that Lowell and Azure allude to the meter reading application, and Jones does not, would not, in my opinion, have made Lowell and Azure more logical choices than Jones to one having ordinary skill in Ambrosio's art in 1976.

E. If it was obvious to one skilled in the art in 1976 to embellish the teachings of Ambrosio, RAM storage would have been the obvious first choice as a storage medium, and one skilled in the Ambrosio art would have recognized this teaching in Jones as well as this teaching in Lowell or Azure.

6. That he has read the Etter patent No. 4,133,034, and believes that the written description of the invention, and of the manner and process of making and using it, are in such full, clear, concise and exact terms that he could have made and used the same based upon his knowledge and experience as of at least July 27, 1977, and this would have been a fairly straightforward task without any undue experimentation.

Michael T. Gray

Michael T. Gray

Dated: 2/23/83

STATE OF CALIFORNIA :
: ss
COUNTY OF SANTA CLARA :

ROSEMARY A. PERRAULT
NOTARY PUBLIC-CALIFORNIA
SANTA CLARA COUNTY
My Commission Exp Aug 6, 1986

On this 23rd day of February, 1983, before me a Notary Public, appeared MICHAEL T. GRAY, ~~to me personally known, and did sign the above document as his free and voluntary act.~~ PROVED TO ME ON THE BASIS OF SATISFACTORY EVIDENCE TO BE THE PERSON WHOSE NAME IS SUBSCRIBED TO THIS INSTRUMENT AND DID SIGN THE ABOVE DOCUMENT AS HIS FREE AND VOLUNTARY ACT.

Rosemary A. Perrault

Notary Public

Donald H. Zarley
ZARLEY, McKEE, THOMTE,
VOORHEES & SEASE
2400 Ruan Center
Des Moines, Iowa 50309
515-288-3667

ATTORNEYS FOR PETITIONER

Office-Supreme Court, U.S.
FILED
JUL 11 1985
ALEXANDER L. STEVAS,
CLERK

No. 84-2003

In the
SUPREME COURT OF THE UNITED STATES

October Term 1984

BERWYN E. ETTER,
Petitioner,

vs.

COMMISSIONER OF PATENTS AND TRADEMARKS,
Respondent,

ANTHONY E. B. GOODFELLOW,
Intervenor.

On Petition to the United States Supreme Court for Writ of Certiorari to the Court of Appeals of the Federal Circuit.

SUPPLEMENTAL APPENDIX

Donald H. Zarley
ZARLEY, McKEE, THOMTE,
VOORHEES & SEASE
2400 Ruan Center
Des Moines, Iowa 50309
515-288-3667

ATTORNEYS FOR PETITIONER

SUPPLEMENTAL APPENDIX

TABLE OF CONTENTS PAGE NO.

Decision of the Board of Appeals of the United States Patent and Trademark Office 1-10

Art Unit 236 Paper No. 37

Appeal No. 556-68 fh

HEARD: January 26, 1984

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF APPEALS

Ex parte Berwyn E. Etter

Request filed February 4, 1982, Control No. 90/000,154, for the Reexamination of Patent No. 4,133,034, issued January 2, 1979, based on application Serial No. 819,350, filed July 27, 1977. Method and Means of Assimilating Utility Meter Data.

Donald H. Zarley et al. for appellant.

Primary Examiner - Errol A. Krass.

Before Bennett, Spencer and Nusbaum, Examiners-in-Chief. Spencer, Examiner-in-Chief.

This appeal is from the decision of the Examiner finally rejecting claims 1 through 9. No other claims are presented.

Claim 1 is illustrative and reads as follows:

1. A method of assimilating utility meter data at the meter locations, comprising,

accumulating on an input information electronic storage means customer profile information for a plurality of meter customers, said profile information including the customer identity and account information,

placing said input information electronic storage means in a portable computer capable of being manually carried to the site of a given meter, said portable computer having an output information storage means and having the capability of updating, printing and presenting various of said customer profile information

for said meter customers before and after receiving current customer profile information,

actuating said computer to segregate and to visually present from the customer profile information for a plurality of meter customers stored on said input information electronic storage means at least the meter number and customer identity information of a given meter customer,

imposing into said computer the current meter reading of said given meter customer at the site of the meter being read,

actuating said computer to calculate the charge for utility usage based upon the previous meter reading and said current meter reading,

actuating said computer to print a bill for said meter customer at the site of said meter based upon said calculation and imposing on said output information storage means the updated customer profile information,

and depositing said bill at the service address of said given meter customer.

The references relied on are:

Boyce	3,654,449	Apr. 4, 1972
Ambrosio	3,932,730	Jan. 13, 1976
Hundley	3,947,665	Mar. 30, 1976
Dallimonti	4,001,807	Jan. 4, 1977
Azure	4,016,542	Apr. 5, 1977
Ng et al. (Ng)	4,025,766	May 24, 1977

Claims 1 through 9 stand rejected under 35 USC 103. As evidence of

obviousness, the Examiner cites Ambrosio and Azure for claims 1, 2, 4, 5 and 9, Ambrosio, Azure and Hundley or Dallimonti for claim 3, Ambrosio, Azure and Boyce for claim 6 and Ambrosio, Azure and Ng for claims 7 and 8.

We make reference to the answer and two supplemental answers for the position of the Examiner and to the brief, reply brief and two supplemental reply briefs for the position of appellant.

O P I N I O N

We have carefully reviewed the entire record before us and have given careful consideration to

appellant's extensive arguments. We find ourselves in full agreement with the Examiner and will affirm the rejections for the reasons set forth by him, as well as our additional comments infra.

Initially, we note that appellant draws no distinction as to patentability between the claims. Accordingly, all of the claims stand or fall together. In re Hellsund, 474 F.2d 1307, 177 USPQ 170 (CCPA 1973).

Appellant urges that the Examiner erred in not disqualifying himself from the instant reexamination proceeding. Appellant asserts that he has been prejudiced by the Examiner's involvement in other interrelated proceedings involving the patent under reexamination.

We fully agree with the Examiner that this is a petitionable rather than an appealable matter. We clearly lack jurisdiction to remand the application to another Examiner as appellant requests. We note, however, that there is nothing in the record which indicates that the Examiner's actions were prejudicial to appellant or that the proceedings below were detrimental to the interests of the public or appellant. The material in the Branning application which appellant considers slanderous is irrelevant to the determination of the obviousness/nonobviousness of the claims at bar over the cited prior art.

Appellant's arguments in traversal of the rejections are largely

predicated on the statutory presumption of validity. Appellant misconstrues the effect of the statutory presumption. The presumption is a procedural device, not substantive law. It does not have separate evidentiary value. Section 282 places the burden of going forward, as well as the burden of persuasion on the party asserting invalidity. Stratoflex Inc. v. Aeroquip Corporation. 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); SSIH Equipment, S.A. v. United States International Trade Commission, 713 F.2d 746, 218 USPQ 678 (Fed. Cir. 1983); Solder Removal Company v. United States International Trade Commission, 582 F.2d 628, 199 USPQ 129 (CCPA 1978). The introduction of new prior art,

whether it be more pertinent or less pertinent than the prior art considered during initial examination, can neither weaken nor strengthen the presumption of validity. The presumption of validity does not act as a shield or render the claims immune to attack by any prior art.

Appellant urges that an increased burden is placed on the Examiner in reexamination proceedings as compared to examination proceedings in view of the presumption of validity. Appellant cites no authority for this proposition and we know of none. In any examination proceeding, the burden of showing nonpatentability is on the Examiner. It is not apparent to us how such a burden can be

increased for reexamination proceedings. The statutes provide, in 35 USC 301, that "reexamination will be conducted according to the procedures established for initial examination under the provisions of sections 132 and 133 of this title." Section 1.550 of 37 CFR provides that examination will be conducted in accordance with sections 1.104-1.119. Sections 1.104-1.119 make no distinctions between examination and reexamination. The scope of reexamination is limited by 37 CFR 1.552 but, except for such limitations, the criteria for determining patentability under sections 102 and 103 are the same for reexamination and initial examination.

Appellant urges that the Examiner had Ambrosio and Jones before him during prosecution of the application which matured into the patent under reexamination and allowed the claims. Apellant further urges that Azure, if not less pertinent than Jones, is at most cumulative to Jones and, if the claims were allowable after a consideration of Ambrosio and Jones, they are allowable in view of Ambrosio and Azure. Appellant asserts that there has not been any satisfactory explanation of why the Examiner considered the claims to be patentable over Ambrosio and Jones in the original application and now considers the claims nonpatentable over Ambrosio and Azure.

We fully agree with the Examiner that Azure is more pertinent than Jones. Azure contains the teaching

"In a typical meter reading application it is required that the meter reader carry information (fixed data) with him related to each stop on his route for that day, including the house number, meter number, previous meter reading, a code for the location of the meter, and warning codes such as for a mad dog. This information can be loaded into the first field of each line of the memory of the electronic notebook from a computer, prior to proceeding on the route. The corresponding line then is displayed in use at each route stop, and the meter reading (variable data) would be entered into a second field."

No such teaching appears in Jones. In our view, the collective teachings of Ambrosio and Azure would have provided a much stronger suggestion for combining the teachings to provide the subject matter of claim 1 than would have the collective teachings of Ambrosio and Jones. Appellant should not construe this as meaning we consider the claims to be unobvious in view of Ambrosio and Jones.

Appellant relies on the affidavit of patentee Ambrosio as evidence that the modification of Ambrosio in view of Azure proposed by the Examiner would not have been obvious. We find the affidavit singularly unpersuasive. Patentee Ambrosio avers that, at the time of filing the application which matured into Ambrosio, "he had

knowledge of the computer concepts of ROM (read only memory) and RAM (random access memory), but it was not obvious to him that these concepts would have any utility in his invention other than as referred to in his patent."

The evidence for obviousness adduced by the Examiner is the collective teachings of Ambrosio and Azure. The combination of the teachings of Ambrosio and knowledge of the computer concepts of ROM and RAM is not the same or equivalent evidence. There is nothing in the evidence relied upon by patentee Ambrosio in arriving at the conclusion of nonobviousness which is equivalent to the Azure teaching that the fixed data required by a meter reader "can be loaded into

the first field of each line of the memory of the electronic notebook from a computer, prior to proceeding on the route."

Patentee Ambrosio also avers that "his appreciation of the ROM and RAM concepts in the fall of 1976 was no greater than at the time he filed his patent application," but says nothing about what was or was not obvious to him in the fall of 1976. This latter averment means hardly anything more than that patentee Ambrosio did not keep up with ROM and RAM developments during the two-year period.

At page 27 of the principal brief, appellant asserts, with respect to column 1, lines 47-60, of Azure (appellant's emphasis), "One having

ordinary skill in the art with knowledge of Ambrosio would learn nothing new from Azure's brief description of Ambrosio for that information was already conveyed by Ambrosio."

There is nothing in Azure to indicate that these lines are a description of Ambrosio. The filing date of Azure is more than 20 months prior to the issue date of Ambrosio. Ambrosio does not convey the information conveyed in these lines of Azure. In particular, Ambrosio does not convey the teaching of loading fixed data into the memory of an electronic notebook prior to the meter reader proceeding on his route. One of ordinary skill in the art would have manifestly learned something new from Azure.

Appellant relies on an affidavit by Gray as evidence of the nonobviousness of the claims at bar in view of Ambrosio and Azure. Gray states that the hardwired discrete logic technology disclosed in Azure was obsolete in the fall of 1976. This is irrelevant. The rejection is not predicated on incorporating the hardwired discrete logic circuitry of Azure into the Ambrosio device. It is based on the suggestion in the collective teachings of Ambrosio and Azure to employ electronic storage means in Ambrosio in lieu of punched cards. The fact that the microprocessor devices of Jones and Lowell would have presented more logical modifications of Ambrosio than would have the hardwire discrete logic based

device of Azure is equally irrelevant. Neither the claims nor the rejections have anything to do with the technology to be employed in modifying Ambrosio in view of Azure.

Gray uses language such as "one of ordinary skill in the art of Ambrosio, if seeking to update the Ambrosio concept, and if having the insight to look to the existing microprocessor art." This demonstrates a total lack of appreciation of the legal concept of obviousness. Obviousness is not determined by what a person of ordinary skill would have done if such a person were seeking to update an earlier concept and if such a person had the insight to look

to the relevant prior art. It is based on what the collective teachings of the relevant prior art would have suggested to a person of ordinary skill in the art who had full knowledge of the relevant prior art. In re Rosselet, 347 F.2d 847, 146 USPQ 183 (CCPA 1965).

The use of the legal term of art "obvious" by Gray, as well as by patentee Ambrosio, can be considered only as it is used in layman's parlance. In re Reuter, 651 F.2d 751, 210 USPQ 249 (CCPA 1981).

The largely irrelevant Gray affidavit is manifestly nonpersuasive.

Appellant's arguments that the lack of method claims in Ambrosio and

Azure is indicative of the nonobviousness of the method claims at bar are predicated on non sequitors. We ignore the remarks regarding Lowell since that reference is not prior art and it, therefore, has no bearing on the obviousness issue. The obviousness determination is based upon what is disclosed in the relevant prior art and what is suggested by the collective disclosures of the relevant prior art. The types of claims which appear in the prior art patents have nothing to do with the determination. Insofar as the claims at bar are concerned, neither Ambrosio nor Azure contains support therefor and such claims could manifestly not have been made in those patents.

Appellant's statement that Ambrosio could have included broad method claims which would have dominated the claims at bar is pure conjecture and not germane.

Appellant urges that none of the prior art includes the step of visually displaying the meter number. Appellant is incorrect. Azure states "[t]he corresponding line [fixed data including the meter number] then is displayed in use at each route stop." Ambrosio provides a visual display of the meter number on the punched card. One of ordinary skill in the art, in modifying Ambrosio in view of Azure to employ electronic storage, would have found it manifestly obvious to provide for display of the meter number.

Our reviewing court has held that claims in a reissue application enjoy no presumption of validity. In re Sneed, 710 F.2d 1544, 218 USPQ 385 (Fed. Cir. 1983). We are not aware of any holding by that court or any other court on the question of whether or not claims in a reexamination proceeding enjoy a presumption of validity. Logically, there seems to be no reason for such a presumption to attach. The presumption is based on the recognized expertise of the Patent and Trademark Office (PTO) and, since that office has made a determination of patentability, a third party should properly have the burden of going forward and the burden of persuasion. No reason is

seen to accord the earlier determination of patentability by the PTO any greater weight than the later determination of nonpatentability by the PTO. We need not, however, decide the question of whether or not a presumption of validity attaches since, even if the claims at bar are accorded a presumption of validity, the Examiner has, in our view, carried any burden imposed by section 282.

C O N C L U S I O N

The rejection of claims 1 through 9 under 35 USC 103 and the decision of the Examiner are affirmed.

AFFIRMED

/s/ Rodney D. Bennett, Jr. Examiner-in-Chief	)
/s/ Richard A. Spencer, Jr. Examiner-in-Chief	) BOARD) OF) APPEALS
/s/ Mark E. Nusbaum Examiner-in-Chief	)

Donald H. Zarley, Esq.
Zarley, McKee, Thomte,
Voorhees & Sease
2400 Ruan Center
Des Moines, Iowa 50309

cc:
Martin Fleit
Fleit & Jacobson
2033 M Street, N.W.
Washington, D C 20036

Donald H. Zarley
ZARLEY, McKEE, THOMTE,
VOORHEES & SEASE
2400 Ruan Center
Des Moines, Iowa 50309
515-288-3667

ATTORNEYS FOR PETITIONER